everyday genius

MT6752 LTE Smartphone Application Processor Technical Brief

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1.0	2014-04-25	Sonic Yang	Initial draft
1.1	2014-05-19	Sonic Yang	Modify gpio mux function
1.2	2014-06-10	Sonic Yang	Modify block diagram

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

The MT6752 device (see ***Figure 1***), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE smart phone applications,. The chip integrates ARM® Cortex-A53 operating up to 1.7GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Octa-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 4, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6752 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6752 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6752

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.7GHz
- LPDDR3 up to 3GB, 800MHz
- LTE Cat 4 (150Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps.
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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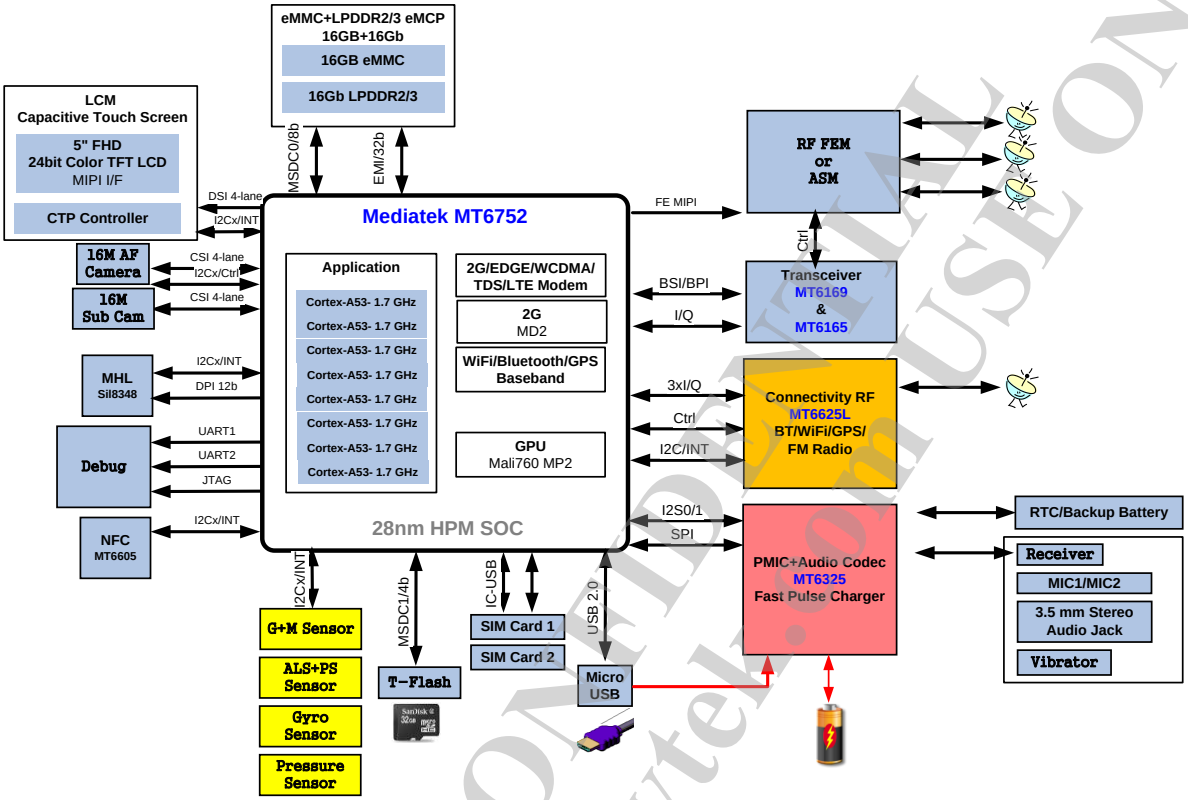

Figure 1. High-level MT6752 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR-2/LPDDR-3

- **AP MCU subsystem**
  - Octa-core ARM® 1.7Ghz Cortex-A53 MPCore™
  - NEON multimedia processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 1MB unified L2 cache
  - DVFS technology with adaptive operating voltage from 0.8V to 1.1V

- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with max. 800 MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks, with max. 300MHz operation frequency
  - FD216 DSP for running modem/voice tasks, with max. 250MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR2/3 up to 3GB
  - Single channel with 32-bit data bus width
  - Memory clock up to 800 MHz
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 HS/FS support
  - IC-USB device mode
  - eMMC5.0
  - 4 UART for debugging and applications
  - SPI master for external device
  - 3 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 4 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.0V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**

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- Type: TFBGA
- 12.6mm*12.6mm
- Height: Max. 0.9mm
- Ball count: 677 balls
- Ball pitch: 0.4mm

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1.3 MODEM Features

- **LTE**
  - FDD: Up to 150Mbps downlink, 50Mbps uplink
  - TDD: Up to 150Mbps downlink, 50Mbps uplink
  - 1.4 to 20MHz RF bandwidth
  - 2*2 downlink SU-MIMO; 4*2 downlink SU-MIMO
  - IPv6, QoS
  - Inter-RAT capabilities with HSPA+, EDGE and applicable backward-compatible modes
  - SNOW3G/ZUC cipher offload engine

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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1.4 Connectivity Features

MT6752 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625. With four advanced radio technologies integrated on one chip, MT6752/MT6625 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4 GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT6752 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated WIFI/BlueTooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)
- **Wi-Fi**
  - Dual-band (2.4GHz/5Ghz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control
- **BlueTooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

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  - Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Support dual-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to FHD (1,920*1,080)
  - MIPI DSI interface (4 data lanes)
  - MiraVision™ for picture quality enhancement
  - ClearMotionTM for DTV-class video quality
  - Embedded LCD gamma correction
  - True colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Wide gamut

- **Graphics**
  - OpenGL ES 3.0 3D graphic accelerator capable of processing 155M tri/sec and 1,400M pixel/sec @ 700MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Integrated image signal processor supports 16MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 16M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture), [16MP + 5MP]@20fps
  - Hardware JPEG encoder: Baseline encoding with 160M pixel/sec. Continuous shot with 96M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps
  - VP9 decoder 1080p @ 30fps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps
  - H.263 encoder: Simple profile D1 @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps
  - HEVC encoder: Main profile 720p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz

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- Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
- Interfaces supported: I2S, PCM
- External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
- 4-band IIR compensation filter to enhance loudspeaker responses
- Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM
- Voice wakeup

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.6 General Description

MediaTek's MT6752 is a highly integrated LTE System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.4, Octa HMP core operating at 1.7GHz, 3D graphics (OpenGL|ES 3.0), 16M camera ISP, LPDDR3-800 Mbps, FHD display and 1080p video codec. MT6752 helps phone manufacturers build high-performance LTE smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6752 is the brand-new generation smart phone SoC integrating MediaTek LTE modem, Octa-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-value Product!

To enrich the camera features, MT6752 equips a 16M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, optical zoom, panorama view, picture in picture, video in video and video face beautification.

Incredible Browser Experience!

The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.0 also provides you with excellent multimedia experiences.

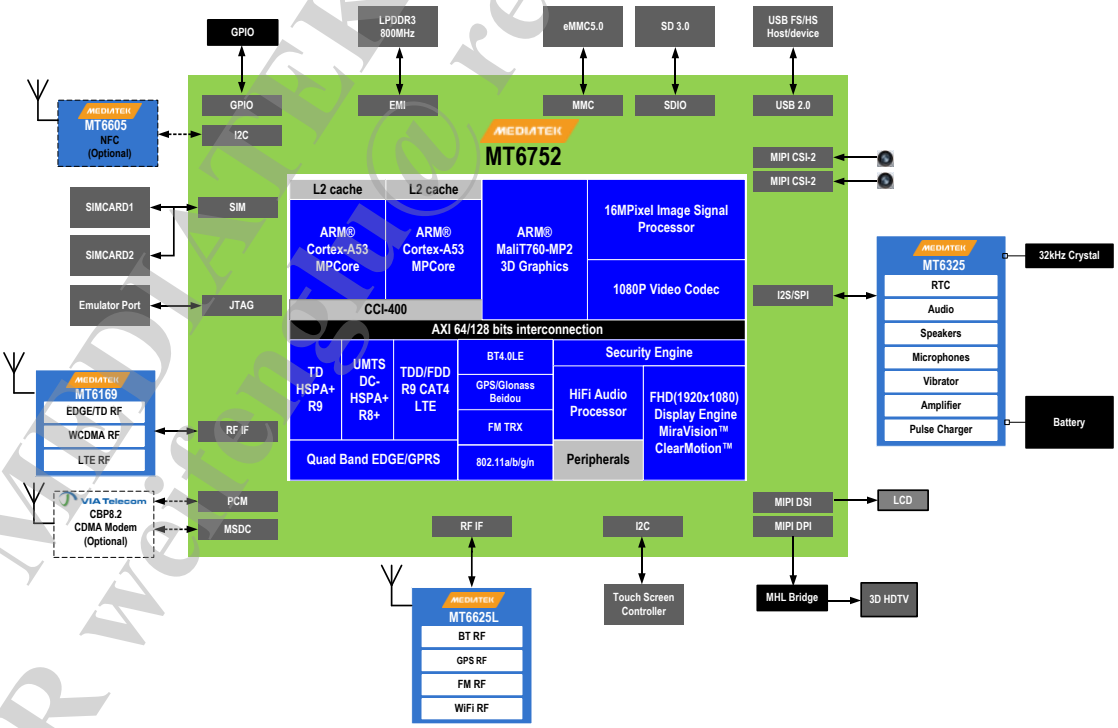

Figure 2. Block diagram of MT6752

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

Figure 3. Ball map view for LPDDR3

2.1.2 Pin Coordinate

Table 1. Pin coordinate (using LPDDR3)

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	GND	M17	GND	AA10	DVDD_DVFS
A2	CS1_N	M18	GND	AA11	DVDD_DVFS
A4	CA4	M19	GND	AA12	DVDD_DVFS
A7	CA0	M20	DVDD_LTE	AA13	GND
A9	DQ16	M21	DVDD_LTE	AA14	GND
A12	DQ22	M22	DVDD_LTE	AA15	GND
A14	DQ2	M23	DVDD_LTE	AA16	GND
A17	DQ7	M24	DVDD_LTE	AA17	GND
A19	DQ9	M27	WB_SDATA	AA18	GND
A22	DQ15	M28	WB_CTRL5	AA19	GND
A24	DQ28	M29	AVSS18_WBG	AA20	DVDD_LTE
A27	DQ30	M30	WB_RXQP	AA21	DVDD_LTE
A29	MSDC0_CLK	M31	WB_RXIN	AA22	DVDD_LTE
A30	MSDC0_DSL	N1	VRT	AA23	DVDD_LTE
A31	GND	N2	TDN1	AA24	DVDD_LTE
B1	CA7	N3	TDP1	AA27	DPI_D5
B2	GND	N4	TDN0	AA30	DPI_D6
B3	CS0_N	N5	AVSS18_MIPITX	AB1	AUD_DAT_MOSI
B4	GND	N7	GND	AB2	AUD_DAT_MISO
B5	CA2	N8	GND	AB3	PWRAP_SPI0_CK
B7	GND	N9	DVDD_GPU	AB4	IDDIG
B8	DQ17	N10	DVDD_GPU	AB5	PWRAP_SPI0_MO
B9	GND	N11	GND	AB7	DVDD_DVFS
B10	DQ20	N12	GND	AB8	DVDD_DVFS
B12	GND	N13	DVDD_GPU	AB9	DVDD_DVFS
B13	DQ0	N14	GND	AB10	DVDD_DVFS
B14	GND	N15	GND	AB11	DVDD_DVFS
B15	DQ4	N16	GND	AB12	DVDD_DVFS
B17	GND	N17	GND	AB13	GND
B18	DQ8	N18	GND	AB14	DVDD_TOP
B19	GND	N19	GND	AB15	DVDD_TOP
B20	DQ11	N20	DVDD_LTE	AB16	DVDD_TOP
B22	GND	N21	DVDD_LTE	AB17	DVDD_TOP
B23	DQ25	N22	DVDD_LTE	AB18	DVDD_TOP
B24	GND	N23	DVDD_LTE	AB19	DVDD_TOP
B25	DQ27	N24	DVDD_LTE	AB20	GND
B27	GND	N27	GND	AB21	GND
B28	MSDC0_DAT0	N28	GND	AB22	GND
B29	MSDC0_DAT1	N30	WB_RSTB	AB23	GND
B30	MSDC0_DAT6	N31	WB_RXIP	AB24	GND
B31	MSDC0_CMD	P1	AVDD18_MIPITX1	AB27	GND
C1	GND	P3	USB_DP_P1	AB28	VOW_CLK_MISO

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C2	CA8	P5	AVDD33_USB_P0	AB29	DPI_D11
C3	CA6	P7	DVDD_SRAM	AB30	DPI_D8
C5	GND	P8	GND	AB31	DPI_D7
C6	CA3	P9	GND	AC2	AUD_CLK_MOSI
C8	DQ18	P10	GND	AC5	PWRAP_SPI0_MI
C10	GND	P11	GND	AC8	DVDD_DVFS
C11	DQ19	P12	GND	AC9	DVDD_DVFS
C13	DQ1	P13	GND	AC10	GND
C15	GND	P14	DVDD_TOP	AC11	GND
C16	DQ6	P15	DVDD_TOP	AC12	GND
C18	DQM1	P16	DVDD_TOP	AC14	DVDD_TOP
C20	GND	P17	DVDD_TOP	AC15	DVDD_TOP
C21	DQ14	P18	DVDD_TOP	AC16	DVDD_TOP
C23	DQM3	P19	GND	AC17	DVDD_TOP
C25	GND	P20	GND	AC18	DVDD_TOP
C26	DQ31	P21	GND	AC19	DVDD_TOP
C27	DQ29	P22	GND	AC20	DVDD_TOP
C29	MSDC0_DAT5	P23	GND	AC21	GND
C30	MSDC0_DAT3	P24	GND	AC22	GND
D1	EXTDN	P27	F2W_DATA	AC23	GND
D2	CA9	P28	F2W_CLK	AC26	CAM_CLK0
D3	GND	P29	AVSS18_WBG	AC27	CMPCLK
D4	CA5	P30	WB_SEN	AC28	CMPDAT1
D5	CKE	P31	AVSS18_WBG	AC29	CMPDAT0
D6	GND	R2	USB_DM_P1	AC30	CAM_PDN1
D7	CA1	R3	CHD_DM_P0	AC31	DVDD18_IO1
D8	GND	R4	CHD_DP_P0	AD1	TESTMODE
D9	DQ21	R5	AVDD33_USB_P1	AD2	WATCHDOG
D10	DQ23	R8	DVDD_DVFS	AD4	GND
D11	GND	R10	DVDD_DVFS	AD5	PWRAP_SPI0_CSN
D12	DQM2	R12	DVDD_DVFS	AD7	DVDD_DVFS
D13	GND	R13	GND	AD10	DVDD_DVFS
D14	DQ3	R14	DVDD_TOP	AD11	DVDD_DVFS
D15	DQ5	R15	DVDD_TOP	AD27	CAM_RST1
D17	DQM0	R16	DVDD_TOP	AD28	CAM_RST0
D18	GND	R17	DVDD_TOP	AD29	CAM_PDN0
D19	DQ10	R18	DVDD_TOP	AE1	DSI_TE
D20	DQ12	R19	GND	AE2	LCM_RST
D21	GND	R20	GND	AE3	RTC32K_CK
D22	DQ13	R21	GND	AE4	SYSRSTB
D23	GND	R22	GND	AE6	DVDD_SRAM
D24	DQ24	R23	GND	AE7	DVDD_DVFS

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D25	GND	R24	GND	AE26	RCP
D26	DQ26	R26	SCL2	AE27	RCN
D27	GND	R27	SDA2	AE30	RDN0
D28	MSDC0_DAT4	R28	SCL1	AE31	RDP0
D29	MSDC0_DAT2	R29	SDA1	AF2	KPCOL1
D30	MSDC0_DAT7	R30	SDA0	AF3	KPROW0
D31	DVDD18_MSDC0	T1	USB_DM_P0	AF4	GND
E1	GND	T2	USB_DP_P0	AF5	GND
E2	GND	T4	USB_VRT_P0	AF15	AVSS18_MD
E3	CLK0_C	T5	AVSS33_USB	AF16	TDX26M_IN
E4	CLK0_T	T6	AVSS18_PLLGP	AF17	AVSS18_MDPLLGP
E5	DDRV	T7	DVDD_DVFS	AF18	TD_RX_BBIN
E6	DDRV	T8	DVDD_DVFS	AF19	TD_RX_BBQN
E7	GND	T9	DVDD_DVFS	AF21	RFIC1_BSI_CK
E8	GND	T10	DVDD_DVFS	AF27	AVSS18_MIPIRX
E9	DQS2_T	T11	DVDD_DVFS	AF28	RDP2
E10	DDRV	T12	DVDD_DVFS	AF29	RDN2
E11	AVSS18_MEMPLL	T13	GND	AF30	RDP1
E12	GND	T14	GND	AF31	RDN1
E13	DQS0_C	T15	GND	AG1	DISP_PWM
E14	DDRV	T16	GND	AG2	KPCOL0
E15	DDRV	T17	GND	AG3	KPROW1
E16	DQS1_C	T18	GND	AG4	GND
E17	GND	T19	GND	AG5	BPI_BUS26
E18	GND	T20	DVDD_LTE	AG6	GND
E19	DQS3_T	T21	DVDD_LTE	AG7	BPI_BUS18
E20	DDRV	T22	DVDD_LTE	AG9	ET_N
E21	DDRV	T23	DVDD_LTE	AG10	ET_P
E22	GND	T24	DVDD_LTE	AG11	LTE_TX_BBIP
E23	GND	T27	SCL3	AG12	LTE_TX_BBQP
E24	VREF_CA	T28	SDA3	AG14	LTEX26M_IN
E25	VREF_AP	T30	SCL0	AG17	AVSS18_MDPLLGP
E26	GND	T31	I2S0_LRCK	AG18	TD_RX_BBIP
E27	GND	U2	AVDD18_USB	AG19	TD_RX_BBQP
E28	MSDC0_RSTB	U4	AVDD18_PLLGP	AG20	GND
E29	GND	U5	TP	AG21	RFIC0_BSI_D2
E30	AVDD18_WBG	U6	TN	AG22	RFIC0_BSI_CK
F1	DVDD28_MSDC1	U7	DVDD_DVFS	AG23	GND
F2	GND	U8	DVDD_DVFS	AG24	BPI_BUS11
F3	GND	U9	DVDD_DVFS	AG25	BPI_BUS8
F4	DDRV_CLK	U10	DVDD_DVFS	AG26	BPI_BUS0
F5	DDRV	U11	DVDD_DVFS	AG29	RCN_A

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F6	DDRV	U12	DVDD_DVFS	AG30	RDN3
F7	GND	U13	GND	AH1	SPI_MO
F8	GND	U14	GND	AH2	PWM_A
F9	DQS2_C	U15	GND	AH3	SRCLKENAI
F10	DDRV	U16	GND	AH5	BPI_BUS27
F11	AVDD18_MEMPLL	U17	GND	AH6	BPI_BUS25
F12	DDRV	U18	GND	AH7	BPI_BUS19
F13	DQS0_T	U19	GND	AH8	BPI_BUS17
F15	DDRV	U20	DVDD_LTE	AH9	AVSS18_MD
F16	DQS1_T	U21	DVDD_LTE	AH11	LTE_TX_BBIN
F17	GND	U22	DVDD_LTE	AH12	LTE_TX_BBQN
F18	GND	U23	DVDD_LTE	AH14	AVSS18_MD
F19	DQS3_C	U24	DVDD_LTE	AH16	APC
F20	DDRV	U26	I2S1_DO	AH17	AVSS18_MDPLLGP
F21	DDRV_VREF	U27	I2S1_LRCK	AH18	AUXIN2
F22	VREF_DQ	U30	I2S0_BCK	AH19	AUXIN1
F30	GPS_RXQN	U31	I2S0_DI	AH21	RFIC0_BSI_D1
F31	GPS_RXQP	V1	DVDD28_SIM2	AH22	RFIC0_BSI_D0
G1	MSDC1_CLK	V2	DVDD18_BIAS3	AH23	BPI_BUS12
G2	MSDC1_DAT3	V7	DVDD_DVFS	AH25	BPI_BUS7
G4	MSDC1_DAT1	V8	DVDD_DVFS	AH26	BPI_BUS6
G12	DDRV	V9	DVDD_DVFS	AH27	BPI_BUS1
G27	AVSS18_WBG	V10	DVDD_DVFS	AH28	AVSS18_MIPIRX
G29	AVSS18_WBG	V11	DVDD_DVFS	AH29	RCP_A
G30	GPS_RXIP	V12	DVDD_DVFS	AH30	RDP3
G31	GPS_RXIN	V13	GND	AH31	RDP0_A
H2	MSDC1_DAT2	V14	DVDD_TOP	AJ1	SPI_CSB
H3	MSDC1_DAT0	V15	DVDD_TOP	AJ2	SPI_MI
H4	MSDC1_CMD	V16	DVDD_TOP	AJ3	MISC_BSI_CS0B
H12	TP_MEMPLL	V17	DVDD_TOP	AJ6	BPI_BUS24
H13	TN_MEMPLL	V18	DVDD_TOP	AJ7	BPI_BUS20
H27	AVSS18_WBG	V19	DVDD_VQPS	AJ8	BPI_BUS16
H28	AVSS18_WBG	V20	GND	AJ9	AVSS18_MD
H29	AVSS18_WBG	V21	GND	AJ14	AVSS18_MD
H30	AVSS18_WBG	V22	GND	AJ16	APC2
J1	SIM1_SCLK	V23	GND	AJ17	AVSS18_MDPLLGP
J2	GND	V24	GND	AJ18	AUXIN0
J4	SIM1_SIO	V26	DPI_VSYNC	AJ19	AVDD18_MDPLLGP
J5	SIM1_SRST	V27	I2S1_BCK	AJ20	RFIC1_BSI_EN
J22	GND	V28	I2S1_MCK	AJ21	RFIC1_BSI_D0
J23	GND	V29	DPI_D9	AJ22	GND
J26	XIN_WBG	V30	I2S0_MCK	AJ23	BPI_BUS13

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
J27	AVSS18_WBG	W1	DVDD28_MD	AJ24	BPI_BUS10
J28	WB_CTRL1	W2	SIM2_SIO	AJ25	BPI_BUS9
J29	WB_CTRL0	W3	SIM2_SCLK	AJ26	BPI_BUS5
J30	WB_TXQN	W4	SIM2_SRST	AJ27	BPI_BUS2
J31	WB_TXQP	W7	GND	AJ28	AVSS18_MIPIRX
K1	DVDD28_SIM1	W8	GND	AJ29	RDN2_A
K2	TDN3	W9	GND	AJ30	RDN1_A
K3	DVDD18_BIAS2	W10	GND	AJ31	RDN0_A
K5	AVSS18_MIPITX	W11	GND	AK1	DVDD18_IO3
K9	DVDD_GPU	W12	GND	AK2	MISC_BSI_DI
K10	DVDD_GPU	W13	DVDD_TOP	AK3	MISC_BSI_CS1B
K11	GND	W14	DVDD_TOP	AK4	MISC_BSI_DO
K12	GND	W15	DVDD_TOP	AK5	MISC_BSI_CK
K13	DVDD_GPU	W16	DVDD_TOP	AK6	BPI_BUS22
K14	DVDD_GPU	W17	DVDD_TOP	AK7	BPI_BUS21
K22	DVDD_TOP	W18	DVDD_TOP	AK9	LTE_RX1_BBIP
K24	DVDD_TOP	W19	DVDD_TOP	AK10	LTE_RX1_BBQP
K26	AVSS18_WBG	W20	GND	AK12	LTE_RX2_BBIP
K28	WB_CTRL2	W21	GND	AK13	LTE_RX2_BBQP
K30	WB_TXIP	W22	GND	AK14	AVSS18_MD
K31	WB_TXIN	W23	GND	AK15	TD_TX_BBIN
L2	TDP3	W24	GND	AK16	TD_TX_BBQN
L5	TCN	W27	DPI_HSYNC	AK18	REFN
L9	DVDD_GPU	W28	DPI_D10	AK20	RFIC1_BSI_D1
L10	DVDD_GPU	W29	DPI_CK	AK22	RFIC0_BSI_EN
L11	GND	W30	DPI_D1	AK23	TD_TXBPI
L12	GND	W31	DPI_D0	AK25	BPI_BUS14
L13	DVDD_GPU	Y2	SRCLKENA0	AK26	BPI_BUS4
L14	DVDD_GPU	Y4	INT_SIM1	AK27	BPI_BUS3
L15	GND	Y5	INT_SIM2	AK28	AVDD18_MIPIRX0
L16	DVDD_TOP	Y7	GND	AK29	RDP2_A
L17	DVDD_TOP	Y8	GND	AK30	RDP1_A
L18	DVDD_TOP	Y9	GND	AL1	DVDD18_IO3
L19	DVDD_TOP	Y10	GND	AL2	SPI_CLK
L20	DVDD_TOP	Y11	GND	AL3	LTE_TXBPI
L21	DVDD_TOP	Y12	GND	AL5	BPI_BUS23
L22	DVDD_TOP	Y13	GND	AL6	BPI_BUS15
L23	DVDD_TOP	Y14	GND	AL8	AVSS18_MD
L24	DVDD_TOP	Y15	GND	AL9	LTE_RX1_BBIN
L27	WB_SCLK	Y16	GND	AL10	LTE_RX1_BBQN
L28	WB_CTRL4	Y17	GND	AL11	AVDD18_MD
L29	WB_CTRL3	Y18	GND	AL12	LTE_RX2_BBIN

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L30	WB_RXQN	Y19	GND	AL13	LTE_RX2_BBQN
M1	TDP2	Y20	DVDD_LTE	AL14	AVDD28_DAC
M2	TDN2	Y21	DVDD_LTE	AL15	TD_TX_BBIP
M3	AVSS18_MIPITX	Y22	DVDD_LTE	AL16	TD_TX_BBQP
M4	TDP0	Y23	DVDD_LTE	AL17	AVDD18_AP
M5	TCP	Y24	DVDD_LTE	AL18	REFP
M7	GND	Y27	DPI_D4	AL20	RFIC1_BSI_D2
M8	GND	Y28	DPI_D2	AL22	DVDD18_IO2
M9	DVDD_GPU	Y30	DPI_D3	AL23	DVDD28_BPI2
M10	DVDD_GPU	Y31	DPI_DE	AL26	DVDD28_BPI1
M11	GND	AA1	DRVBUS	AL27	DVDD18_BIAS1
M12	GND	AA2	SRCLKENA1	AL28	AVDD18_MIPIRX1
M13	DVDD_GPU	AA5	GND	AL29	RDP3_A
M14	DVDD_GPU	AA7	DVDD_DVFS	AL30	RDN3_A
M15	GND	AA8	DVDD_DVFS	AL31	AVSS18_MIPIRX
M16	GND	AA9	DVDD_DVFS		

2.1.3 Detailed Pin Description

Table 2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. Detailed pin description (using LPDDR3)

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DIO	System reset input	DVDD18_IO3
WATCHDOG	DO	Watchdog reset output	DVDD18_IO3
TESTMODE	DIO	Test mode	DVDD18_IO3
RTC32K_CK	DIO	RTC 32K input	DVDD18_IO3
SRCLKENA0	DIO		DVDD18_IO3
SRCLKENA1	DIO		DVDD18_IO3
SRCLKENAI	DIO		DVDD18_IO3

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Pin name	Type	Description	Power domain
PMIC			
PWRAP_SPIo_MO	DIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_SPIo_MI	DIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_SPIo_CSN	DIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_SPIo_CK	DIO	PMIC SPI control interface	DVDD18_IO3
VOW_CLK_MISO	DIO	PMIC SPI control interface	DVDD18_IO1
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD18_IO3
AUD_DAT_MISO	DIO	PMIC audio input interface	DVDD18_IO3
AUD_DAT_MOSI	DIO	PMIC audio input interface	DVDD18_IO3
SIM			
SIM1_SCLK	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SIO	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SRST	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM2_SCLK	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SIO	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SRST	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
INT_SIM1	DIO	SIM1 interrupt	DVDD28_MD
INT_SIM2	DIO	SIM2 interrupt	DVDD28_MD
LCD			
	DIO	Parallel display interface chip	DVDD18_IO1
DSI_TE	DIO	Parallel display interface tearing effect	DVDD18_IO1
LCM_RST	DIO	Parallel display interface reset signal	DVDD18_IO1
DPI_HSYNC	DIO	Parallel display interface HSYNC	DVDD18_IO1
DPI_VSYNC	DIO	Parallel display interface VSYNC	DVDD18_IO1
DPI_CK	DIO	Parallel display interface CLK	DVDD18_IO1
DPI_DE	DIO	Parallel display interface DE	DVDD18_IO1
DPI_D11	DIO	Data pin 11 for DPI parallel LCD interface	DVDD18_IO1
DPI_D10	DIO	Data pin 10 for DPI parallel LCD interface	DVDD18_IO1
DPI_D9	DIO	Data pin 9 for DPI parallel LCD interface	DVDD18_IO1
DPI_D8	DIO	Data pin 8 for DPI parallel LCD interface	DVDD18_IO1
DPI_D7	DIO	Data pin 7 for DPI parallel LCD interface	DVDD18_IO1
DPI_D6	DIO	Data pin 6 for DPI parallel LCD interface	DVDD18_IO1
DPI_D5	DIO	Data pin 5 for DPI parallel LCD interface	DVDD18_IO1
DPI_D4	DIO	Data pin 4 for DPI parallel LCD interface	DVDD18_IO1
DPI_D3	DIO	Data pin 3 for DPI parallel LCD interface	DVDD18_IO1
DPI_D2	DIO	Data pin 2 for DPI parallel LCD interface	DVDD18_IO1
DPI_D1	DIO	Data pin 1 for DPI parallel LCD interface	DVDD18_IO1
DPI_D0	DIO	Data pin 0 for DPI parallel LCD interface	DVDD18_IO1
PWM			
PWM_A	DIO	PWM_A	DVDD18_IO3
DISP_PWM	DIO	Display PWM	DVDD18_IO3
Keypad Interface			

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Pin name	Type	Description	Power domain
KCOL0	DIO	Keypad column 0	DVDD18_IO3
KCOL1	DIO	Keypad column 1	DVDD18_IO3
KROW0	DIO	Keypad row 0	DVDD18_IO3
KROW1	DIO	Keypad row 1	DVDD18_IO3
I2S Interface			
I2S0_BCK	DIO	I2S0_BCK	DVDD18_IO3
I2S0_DI	DIO	I2S0_DI	DVDD18_IO3
I2S0_LRCK	DIO	I2S0_LRCK	DVDD18_IO3
I2S0_MCK	DIO	I2S0_MCK	DVDD18_IO3
I2S1_BCK	DIO	I2S1_BCK	DVDD18_IO3
I2S1_DO	DIO	I2S1_DO	DVDD18_IO3
I2S1_LRCK	DIO	I2S1_LRCK	DVDD18_IO3
I2S1_MCK	DIO	I2S1_MCK	DVDD18_IO3
SPI			
SPI_CSB	DIO	SPI chip select	DVDD18_IO3
SPI_MI	DIO	SPI data in	DVDD18_IO3
SPI_MO	DIO	SPI data out	DVDD18_IO3
SPI_CLK	DIO	SPI clock	DVDD18_IO3
BPI			
BPI_BUS0	DIO	BPI_BUS0	DVDD28_BPI1
BPI_BUS1	DIO	BPI_BUS1	DVDD28_BPI1
BPI_BUS2	DIO	BPI_BUS2	DVDD28_BPI1
BPI_BUS3	DIO	BPI_BUS3	DVDD28_BPI1
BPI_BUS4	DIO	BPI_BUS4	DVDD28_BPI1
BPI_BUS5	DIO	BPI_BUS5	DVDD28_BPI1
BPI_BUS6	DIO	BPI_BUS6	DVDD28_BPI2
BPI_BUS7	DIO	BPI_BUS7	DVDD28_BPI2
BPI_BUS8	DIO	BPI_BUS8	DVDD28_BPI2
BPI_BUS9	DIO	BPI_BUS9	DVDD28_BPI2
BPI_BUS10	DIO	BPI_BUS10	DVDD18_IO2
BPI_BUS11	DIO	BPI_BUS11	DVDD18_IO2
BPI_BUS12	DIO	BPI_BUS12	DVDD18_IO2
BPI_BUS13	DIO	BPI_BUS13	DVDD18_IO2
BPI_BUS14	DIO	BPI_BUS14	DVDD18_IO2
BPI_BUS15	DIO	BPI_BUS15	DVDD18_IO3
BPI_BUS16	DIO	BPI_BUS16	DVDD18_IO3
BPI_BUS17	DIO	BPI_BUS17	DVDD18_IO3
BPI_BUS18	DIO	BPI_BUS18	DVDD18_IO3
BPI_BUS19	DIO	BPI_BUS19	DVDD18_IO3
BPI_BUS20	DIO	BPI_BUS20	DVDD18_IO3
BPI_BUS21	DIO	BPI_BUS21	DVDD18_IO3
BPI_BUS22	DIO	BPI_BUS22	DVDD18_IO3
BPI_BUS23	DIO	BPI_BUS23	DVDD18_IO3

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Pin name	Type	Description	Power domain
BPI_BUS24	DIO	BPI_BUS24	DVDD18_IO3
BPI_BUS25	DIO	BPI_BUS25	DVDD18_IO3
BPI_BUS26	DIO	BPI_BUS26	DVDD18_IO3
BPI_BUS27	DIO	BPI_BUS27	DVDD18_IO3
LTE_TXBPI	DIO	LTE_TXBPI	DVDD18_IO3
TD_TXBPI	DIO	TD_TXBPI	DVDD18_IO2
BSI			
RFIC0_BSI_CK	DIO	RFIC0 BSI CLK	DVDD18_IO2
RFIC0_BSI_D0	DIO	RFIC0 BSI DATA0	DVDD18_IO2
RFIC0_BSI_D1	DIO	RFIC0 BSI DATA1	DVDD18_IO2
RFIC0_BSI_D2	DIO	RFIC0 BSI DATA2	DVDD18_IO2
RFIC0_BSI_EN	DIO	RFIC0 BSI CS	DVDD18_IO2
RFIC1_BSI_CK	DIO	RFIC1 BSI CLK	DVDD18_IO2
RFIC1_BSI_D0	DIO	RFIC1 BSI DATA0	DVDD18_IO2
RFIC1_BSI_D1	DIO	RFIC1 BSI DATA1	DVDD18_IO2
RFIC1_BSI_D2	DIO	RFIC1 BSI DATA2	DVDD18_IO2
RFIC1_BSI_EN	DIO	RFIC1 BSI CS	DVDD18_IO2
MISC_BSI_CK	DIO	RFIC2 BSI CLK	DVDD18_IO3
MISC_BSI_CS0B	DIO	RFIC2 BSI CS0	DVDD18_IO3
MISC_BSI_CS1B	DIO	RFIC2 BSI CS1	DVDD18_IO3
MISC_BSI_DI	DIO	RFIC2 BSI DI	DVDD18_IO3
MISC_BSI_DO	DIO	RFIC2 BSI DO	DVDD18_IO3
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD28_MSDC1
MSDC0			
MSDC0_CLK	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD18_MSDC0
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	DIO	MSDC0 Reset pin	DVDD18_MSDC0
EFUSE			

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Pin name	Type	Description	Power domain
DVDD_VQPS	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI			
DQ0	DIO	DRAM interface	DDRV
DQ1	DIO	DRAM interface	DDRV
DQ2	DIO	DRAM interface	DDRV
DQ3	DIO	DRAM interface	DDRV
DQ4	DIO	DRAM interface	DDRV
DQ5	DIO	DRAM interface	DDRV
DQ6	DIO	DRAM interface	DDRV
DQ7	DIO	DRAM interface	DDRV
DQ8	DIO	DRAM interface	DDRV
DQ9	DIO	DRAM interface	DDRV
DQ10	DIO	DRAM interface	DDRV
DQ11	DIO	DRAM interface	DDRV
DQ12	DIO	DRAM interface	DDRV
DQ13	DIO	DRAM interface	DDRV
DQ14	DIO	DRAM interface	DDRV
DQ15	DIO	DRAM interface	DDRV
DQ16	DIO	DRAM interface	DDRV
DQ17	DIO	DRAM interface	DDRV
DQ18	DIO	DRAM interface	DDRV
DQ19	DIO	DRAM interface	DDRV
DQ20	DIO	DRAM interface	DDRV
DQ21	DIO	DRAM interface	DDRV
DQ22	DIO	DRAM interface	DDRV
DQ23	DIO	DRAM interface	DDRV
DQ24	DIO	DRAM interface	DDRV
DQ25	DIO	DRAM interface	DDRV
DQ26	DIO	DRAM interface	DDRV
DQ27	DIO	DRAM interface	DDRV
DQ28	DIO	DRAM interface	DDRV
DQ29	DIO	DRAM interface	DDRV
DQ30	DIO	DRAM interface	DDRV
DQ31	DIO	DRAM interface	DDRV
DQM0	DIO	DRAM interface	DDRV
DQM1	DIO	DRAM interface	DDRV
DQM2	DIO	DRAM interface	DDRV
DQM3	DIO	DRAM interface	DDRV
DQS0_C	DIO	DRAM interface	DDRV
DQS0_T	DIO	DRAM interface	DDRV
DQS1_C	DIO	DRAM interface	DDRV
DQS1_T	DIO	DRAM interface	DDRV
DQS2_C	DIO	DRAM interface	DDRV

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Pin name	Type	Description	Power domain
DQS2_T	DIO	DRAM interface	DDRV
DQS3_C	DIO	DRAM interface	DDRV
DQS3_T	DIO	DRAM interface	DDRV
CA0	DIO	DRAM interface	DDRV
CA1	DIO	DRAM interface	DDRV
CA2	DIO	DRAM interface	DDRV
CA3	DIO	DRAM interface	DDRV
CA4	DIO	DRAM interface	DDRV
CA5	DIO	DRAM interface	DDRV
CA6	DIO	DRAM interface	DDRV
CA7	DIO	DRAM interface	DDRV
CA8	DIO	DRAM interface	DDRV
CA9	DIO	DRAM interface	DDRV
CKE	DIO	DRAM interface	DDRV
CLK0_C	DIO	DRAM interface	DDRV_CLK
CLK0_T	DIO	DRAM interface	DDRV_CLK
CS0_N	DIO	DRAM interface	DDRV
CS1_N	DIO	DRAM interface	DDRV
VREF_AP	DIO	DRAM interface	DDRV_VREF
VREF_CA	DIO	DRAM interface	DDRV_VREF
VREF_DQ	DIO	DRAM interface	DDRV_VREF
EXTDN	DIO	DRAM interface	DDRV
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_IO1
CAM_CLKO	DIO	Master clock to sensor	DVDD18_IO1
CMPDAT0	DIO	Pixel data[0] from sensor	DVDD18_IO1
CMPDAT1	DIO	Pixel data[1] from sensor	DVDD18_IO1
CAM_RST1	DIO	Reset control to 1st sensor	DVDD18_IO1
CAM_PDN1	DIO	Power down to 1st sensor	DVDD18_IO1
CMPCLK	DIO	Reset control to 2nd sensor	DVDD18_IO1
CAM_CLKO	DIO	Power down to 2nd sensor	DVDD18_IO1
I2C			
SCL0	DIO	I2C0 clock	DVDD18_IO1
SCL1	DIO	I2C1 clock	DVDD18_IO1
SCL2	DIO	I2C2 clock	DVDD18_IO1
SCL3	DIO	I2C3 clock	DVDD18_IO1
SDA0	DIO	I2C0 data	DVDD18_IO1
SDA1	DIO	I2C1 data	DVDD18_IO1
SDA2	DIO	I2C2 data	DVDD18_IO1
SDA3	DIO	I2C3 data	DVDD18_IO1
CONN			
WB_CTRL0	DIO	WB control for CONN_RF	DVDD18_IO1
WB_CTRL1	DIO	WB control for CONN_RF	DVDD18_IO1

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Pin name	Type	Description	Power domain
WB_CTRL2	DIO	WB control for CONN_RF	DVDD18_IO1
WB_CTRL3	DIO	WB control for CONN_RF	DVDD18_IO1
WB_CTRL4	DIO	WB control for CONN_RF	DVDD18_IO1
WB_CTRL5	DIO	WB control for CONN_RF	DVDD18_IO1
WB_RSTB	DIO	Reset for CONN_RF	DVDD18_IO1
WB_SEN	DIO	SPI for CONN_RF	DVDD18_IO1
WB_SCLK	DIO	SPI for CONN_RF	DVDD18_IO1
WB_SDATA	DIO	SPI for CONN_RF	DVDD18_IO1
F2W_CLK	DIO	AUD_IN from CONN_RF	DVDD18_IO1
F2W_DATA	DIO	AUD_IN from CONN_RF	DVDD18_IO1
ABB			
TD_TX_BBIN	AIO	TD_TX_BBIN	AVDD18_MD
TD_TX_BBIP	AIO	TD_TX_BBIP	AVDD18_MD
TD_TX_BBQN	AIO	TD_TX_BBQN	AVDD18_MD
TD_TX_BBQP	AIO	TD_TX_BBQP	AVDD18_MD
LTE_TX_BBIN	AIO	LTE_TX_BBIN	AVDD18_MD
LTE_TX_BBIP	AIO	LTE_TX_BBIP	AVDD18_MD
LTE_TX_BBQN	AIO	LTE_TX_BBQN	AVDD18_MD
LTE_TX_BBQP	AIO	LTE_TX_BBQP	AVDD18_MD
APC	AIO	Automatic power control for modem	AVDD18_MD
APC2	AIO	Automatic power control for modem	AVDD18_MD
LTEX26M_IN	AIO	26MHz clock input for AP and modem	AVDD18_MD
TDX26M_IN	AIO		AVDD18_MD
TD_RX_BBIN	AIO	TD_RX_BBIN	AVDD18_MD
TD_RX_BBIP	AIO	TD_RX_BBIP	AVDD18_MD
TD_RX_BBQN	AIO	TD_RX_BBQN	AVDD18_MD
TD_RX_BBQP	AIO	TD_RX_BBQP	AVDD18_MD
LTE_RX1_BBIN		LTE_RX1_BBIN	AVDD18_MD
LTE_RX1_BBIP		LTE_RX1_BBIP	AVDD18_MD
LTE_RX1_BBQN		LTE_RX1_BBQN	AVDD18_MD
LTE_RX1_BBQP		LTE_RX1_BBQP	AVDD18_MD
LTE_RX2_BBIN	AIO	LTE_RX2_BBIN	AVDD18_MD
LTE_RX2_BBIP	AIO	LTE_RX2_BBIP	AVDD18_MD
LTE_RX2_BBQN	AIO	LTE_RX2_BBQN	AVDD18_MD
LTE_RX2_BBQP	AIO	LTE_RX2_BBQP	AVDD18_MD
REFN	AIO	Negative reference port for internal circuit	AVDD18_MD
REFP	AIO	Positive reference port for internal circuit	AVDD18_MD
AUX_IN0	AIO	AuxADC external input channel 0	AVDD18_MD
AUX_IN1	AIO	AuxADC external input channel 1	AVDD18_MD
AUX_IN2	AIO	AuxADC external input channel 2	AVDD18_MD
ET_N	AIO	Envelope tracking	AVDD18_MD
ET_P	AIO	Envelope tracking	AVDD18_MD
MIPI			

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Pin name	Type	Description	Power domain
TDN0	AIO	DSI0 lane 0 N	AVDD18_MIPITX1
TDP0	AIO	DSI lane 0 P	AVDD18_MIPITX1
TDN1	AIO	DSI lane 1 N	AVDD18_MIPITX1
TDP1	AIO	DSI0 lane 1 P	AVDD18_MIPITX1
TDN2	AIO	DSI0 lane 2 N	AVDD18_MIPITX1
TDP2	AIO	DSI0 lane 2 P	AVDD18_MIPITX1
TDN3	AIO	DSI0 lane 3 N	AVDD18_MIPITX1
TDP3	AIO	DSI0 lane 3 P	AVDD18_MIPITX1
TCN	AIO	DSI0 CK lane N	AVDD18_MIPITX1
TCP	AIO	DSI0 CK lane P	AVDD18_MIPITX1
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	AVDD18_MIPITX1
RDN0	AIO	CSI0 lane0 N	AVDD18_MIPIRX0
RDP0	AIO	CSI0 lane0 P	AVDD18_MIPIRX0
RDN1	AIO	CSI0 lane1 N	AVDD18_MIPIRX0
RDP1	AIO	CSI0 lane 1 P	AVDD18_MIPIRX0
RDN2	AIO	CSI0 lane2 N	AVDD18_MIPIRX0
RDP2	AIO	CSI0 lane2 P	AVDD18_MIPIRX0
RDN3	AIO	CSI0 lane3 N	AVDD18_MIPIRX0
RDP3	AIO	CSI0 lane3 P	AVDD18_MIPIRX0
RCN	AIO	CSI0 CK lane N	AVDD18_MIPIRX0
RCP	AIO	CSI0 CK lane P	AVDD18_MIPIRX0
RDN0_A	AIO	CSI1 lane 0 N	AVDD18_MIPIRX1
RDP0_A	AIO	CSI1 lane 0 P	AVDD18_MIPIRX1
RDN1_A	AIO	CSI1 lane 1 N	AVDD18_MIPIRX1
RDP1_A	AIO	CSI1 lane 1 P	AVDD18_MIPIRX1
RDN2_A	AIO	CSI1 lane 2 N	AVDD18_MIPIRX1
RDP2_A	AIO	CSI1 lane 2 P	AVDD18_MIPIRX1
RDN3_A	AIO	CSI1 lane 3 N	AVDD18_MIPIRX1
RDP3_A	AIO	CSI1 lane 3 P	AVDD18_MIPIRX1
RCN_A	AIO	CSI1 CK lane N	AVDD18_MIPIRX1
RCP_A	AIO	CSI1 CK lane P	AVDD18_MIPIRX1
USB			
USB_DM_P0	AIO	USB D+ differential data line	AVDD33_USB_P0
USB_DP_P0	AIO	USB D- differential data line	AVDD33_USB_P0
USB_DM_P1	AIO	USB D+ differential data line	AVDD33_USB_P1
USB_DP_P1	AIO	USB D- differential data line	AVDD33_USB_P1
CHD_DM_P0	AIO	BC1.1 charger DP	AVDD33_USB_P0
CHD_DP_P0	AIO	BC1.1 charger DM	AVDD33_USB_P0
USB_VRT_P0	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
WBG			
WB_RX_QN	AIO	RX_QN for WIFI/BT Rx	AVDD18_WBG
WB_RX_QP	AIO	RX_QP for WIFI/BT Rx	AVDD18_WBG

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Pin name	Type	Description	Power domain
WB_RX_IP	AIO	RX_IN for WIFI/BT Rx	AVDD18_WBG
WB_RX_IN	AIO	RX_IP for WIFI/BT Rx	AVDD18_WBG
WB_TX_QP	AIO	TX_QP for WIFI/BT Tx	AVDD18_WBG
WB_TX_QN	AIO	TX_QN for WIFI/BT Tx	AVDD18_WBG
WB_TX_IN	AIO	TX_IN for WIFI/BT Tx	AVDD18_WBG
WB_TX_IP	AIO	TX_IP for WIFI/BT Tx	AVDD18_WBG
GPS_RXQN	AIO	RX_QN for GPS Rx	AVDD18_WBG
GPS_RXQP	AIO	RX_QP for GPS Rx	AVDD18_WBG
GPS_RXIP	AIO	RX_IN for GPS Rx	AVDD18_WBG
GPS_RXIN	AIO	RX_IP for GPS Rx	AVDD18_WBG
XIN_WBG	AIO	26MHz clock input for WBG	AVDD18_WBG
MISC			
DRVBUS	DIO	USB OTG	
IDDIG	DIO	USB OTG	
TN	AIO	Reserved	
TP	AIO	Reserved	
TN_MEMPLL	AIO	Reserved	
TP_MEMPLL	AIO	Reserved	
Analog Power			
AVDD18_AP	P	Analog power input 1.8V	
AVDD18_MD	P	Analog power input 1.8V for modem	
AVDD18_MDPLLGP	P	Analog power input 1.8V for PLL	
AVDD18_MEMPLL	P	Analog power input 2.8V for PLL	
AVDD18_MIPIRX0	P	Analog power for MIPI CSI	
AVDD18_MIPIRX1	P	Analog power for MIPI CSI	
AVDD18_MIPITX1	P	Analog power for MIPI	
AVDD18_PLLGP	P	Analog power 1.8V for PLL	
AVDD18_USB	P	Analog power 1.8V for USB	
AVDD18_WBG	P	Analog power 1.8V for WBG	
AVDD28_DAC	P	Analog power 1.8V for DAC	
AVDD33_USB_P0	P	Analog power 1.8V for USB	
AVDD33_USB_P1	P	Analog power 1.8V for USB	
Digital Power			
DDRV	P	Digital power input for DDR	-
DDRV_CLK	P	Digital power input for DDR	-
DDRV_VREF	P	Digital power input for DDR	-
DVDD_DVFS	P	Digital power input for DVFS	-
DVDD_GPU	P	Digital power input for GPU	-
DVDD_LTE	P	Digital power input for LTE	-
DVDD_SRAM	P	Digital power input for SRAM	-
DVDD_TOP	P	Digital power input for TOP	-
DVDD18_BIAS1	P	Digital power input for DDR	-
DVDD18_BIAS2	P	Digital power input for DDR	-

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Pin name	Type	Description	Power domain
DVDD18_BIAS3	P	Digital power input for DDR	-
DVDD18_IO1	P	Digital power input for IO	-
DVDD18_IO2	P	Digital power input for IO	
DVDD18_IO3	P	Digital power input for IO	
DVDD18_MSDC0	P	Digital power input for MSDC0	
DVDD28_BPI1	P	Digital power input for BPI1	
DVDD28_BPI2	P	Digital power input for BPI2	
DVDD28_MD	P	Digital power input for MD	
DVDD28_MSDC1	P	Digital power input for MSDC1	
DVDD28_SIM1	P	Digital power input for SIM1	
DVDD28_SIM2	P	Digital power input for SIM2	
Analog Ground			
AVSS18_MD	G	Analog ground input for modem	
AVSS18_MDPLLGP	G	Analog ground input for PLL	
AVSS18_MEMPLL	G	Analog ground input for PLL	
AVSS18_MIPIRX	G	Analog ground input for MIPI RX	
AVSS18_MIPITX	G	Analog ground input for MIPI TX	
AVSS18_PLLGP	G	Analog ground input for PLL	
AVSS18_WBG	G	Analog ground input for WBG	
AVSS33_USB	G	Analog ground input for USB	
Digital Ground			
GND	G		-

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 4. Acronym for the table of state of pins

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Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
eMMC Interface						
MSDC0_CLK	LO	1	-	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_CMD	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT0	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT1	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT2	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT3	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT4	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT5	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT6	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT7	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_RSTB	HO	1	-	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DSL	I	1	PD	DIOH4,DIOL4	No Need	IO Type 4
SD Card Interface						
MSDC1_CLK	LO	1	-	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_CMD	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT0	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT1	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT2	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT3	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
SIM Interface						
SIM1_SCLK	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM1_SRST	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM1_SIO	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SCLK	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SRST	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SIO	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
Audio Interface						
AUD_CLK_MOSI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
AUD_DAT_MISO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
AUD_DAT_MOSI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
VOW_CLK_MISO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LCD Control						
DISP_PWM	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LCM_RST	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
DSI_TE	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM Interface						
CAM_CLK0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM_RST0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM_RST1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM_PDN0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM_PDN1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CMPCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

[1] The column "State" of "Reset" shows the pin state during reset (Input, High Output, Low Output, etc).
[2] The column "Aux" for "Reset" means the default aux. funtion number shown in Table "Pin Multiplexing, Capability and Settings".
[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

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Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
CMPDAT0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CMPDAT1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PMIC SPI Interface						
PWRAP_SPI0_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_CSN	I	0	PU	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_MI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_MO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2C Interface						
SCL0	I	1	NP	DIOH3,DIOL3	No Need	IO Type 3
SCL1	I	1	NP	DIOH3,DIOL3	No Need	IO Type 3
SCL2	I	1	PD	DIOH1,DIOL1	No Need	IO Type 1
SCL3	I	1	NP	DIOH3,DIOL3	No Need	IO Type 3
SDA0	I	1	NP	DIOH3,DIOL3	No Need	IO Type 3
SDA1	I	1	NP	DIOH3,DIOL3	No Need	IO Type 3
SDA2	I	1	PD	DIOH1,DIOL1	No Need	IO Type 1
SDA3	I	1	NP	DIOH3,DIOL3	No Need	IO Type 3
RFIC Interface						
RFIC0_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_D1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_D2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
MISC_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
MISC_BSI_DO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
MISC_BSI_DI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
MISC_BSI_CS0B	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
MISC_BSI_CS1B	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI Interface						
BPI_BUS0	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS1	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS2	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS3	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS4	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS5	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS6	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS7	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS8	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS9	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS10	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS11	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS12	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS13	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS14	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS15	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS16	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

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Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
BPI_BUS17	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS18	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS19	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS20	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS21	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS22	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS23	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS24	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS25	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS26	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS27	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LTE_TXBPI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
TD_TXBPI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
Connectivity RF Interface						
WB_CTRL0	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
WB_CTRL1	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
WB_CTRL2	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
WB_CTRL3	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
WB_CTRL4	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
WB_CTRL5	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
F2W_DATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
F2W_CLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SEN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_RSTB	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
Keypad						
KPCOL0	I	0	PU	DIOH1,DIOL1	No Need	IO Type 1
KPCOL1	I	0	PU	DIOH1,DIOL1	No Need	IO Type 1
KPROW0	LO	1	-	DIOH1,DIOL1	No Need	IO Type 1
KPROW1	I	0	PU	DIOH1,DIOL1	No Need	IO Type 1
DPI Interface						
DPI_D0	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D1	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D2	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D3	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D4	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D5	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D6	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D7	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D8	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D9	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D10	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D11	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_DE	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_CK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_HSYNC	I	0	PU	DIOH2,DIOL2	No Need	IO Type 2
DPI_VSYNC	I	0	PU	DIOH2,DIOL2	No Need	IO Type 2
I2S Interface						
I2S0_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

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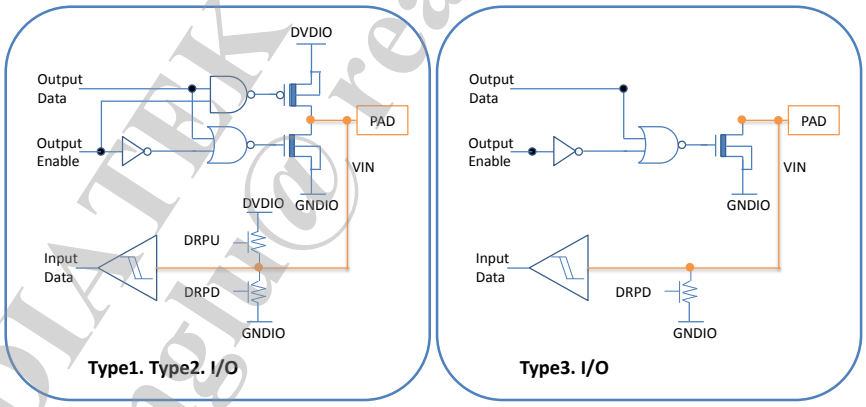
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
I2S0_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_DI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S1_MCK	I	2	PU	DIOH1,DIOL1	No Need	IO Type 1
I2S1_BCK	HO	2	-	DIOH1,DIOL1	No Need	IO Type 1
I2S1_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S1_DO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI Interface						
SPI_CSB	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_CLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_MO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_MI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
System /Reset Clock Enable						
WATCHDOG	HO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENA0	HO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENA1	LO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENAI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWM_A	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
IDDIG	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
DRVBUS	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
INT_SIM1	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
INT_SIM2	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5

Table 5. State of pins



Type1. GPIO 28 type (2mA, 4mA, 6mA, 8mA)
Type2. GPIO 4G type (4mA, 8mA, 12mA, 16mA)

Type 3. Open-drain IO

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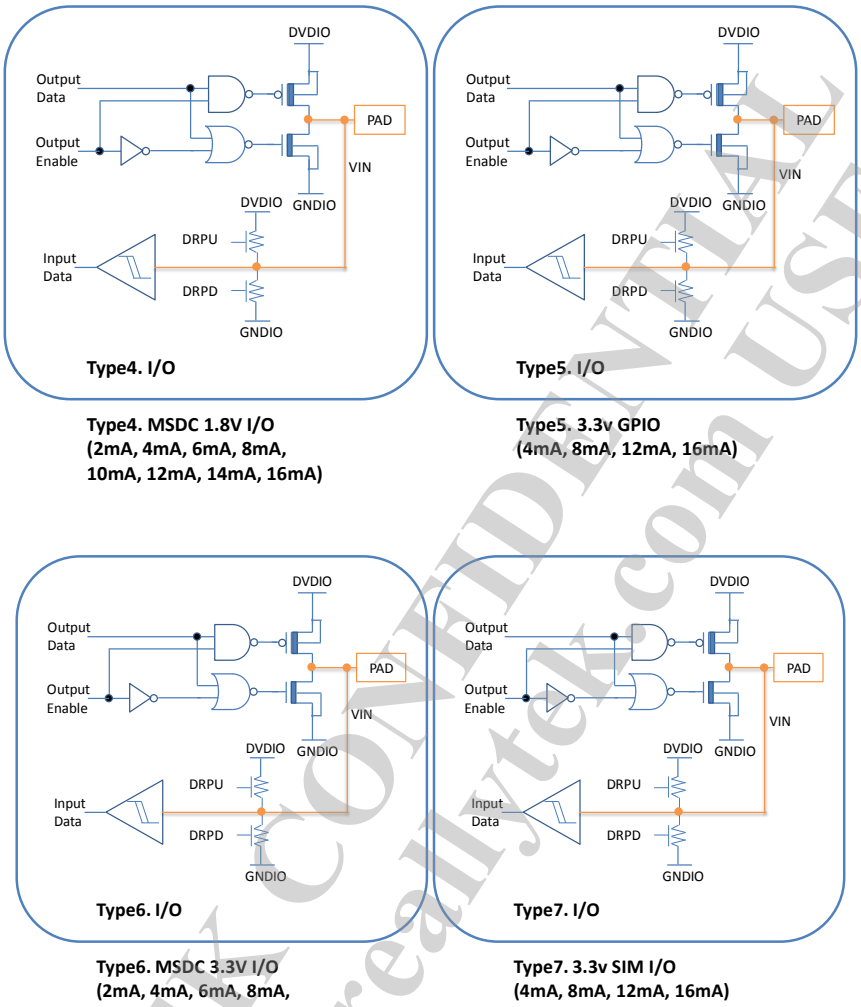

Type4. MSDC 1.8V I/O (2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA)

Type5. 3.3v GPIO (4mA, 8mA, 12mA, 16mA)

Type6. MSDC 3.3V I/O (2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA)

Type7. 3.3v SIM I/O (4mA, 8mA, 12mA, 16mA)

Figure 4. IO types in state of pins

2.1.4 Pin Multiplexing, Capability and Settings

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-dowm

Table 6. Acronym for pull-up and pull-down type

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU /CD	Driving	SMT
MSDC0_CLK	0	GPIO0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_CMD	0	GPIO1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT0	0	GPIO2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT1	0	GPIO3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT2	0	GPIO4	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT3	0	GPIO5	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT4	0	GPIO6	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT4	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT5	0	GPIO7	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT5	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT6	0	GPIO8	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT6	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT7	0	GPIO9	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT7	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_RSTB	0	GPIO10	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_RSTB	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DSL	0	GPIO11	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DSL	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_CLK	0	GPIO12	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD32_JTAG_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	MD2_CLKM0	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A26	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_CMD	0	GPIO13	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD32_JTAG_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	MD2_CLKM1	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A27	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT0	0	GPIO14	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD32_JTAG_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	MD2_URXD	I	CU, CD	2/4/6/8/10/12/14/16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU /CD	Driving	SMT
	5	CONN_DSP_JDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A28	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT1	0	GPIO15	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD32_JTAG_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	MD2_UTXD	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JDO	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A29	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT2	0	GPIO16	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD32_JTAG_TRST	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	CORESONIC_SWCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JINTP	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TRSTN	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A30	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT3	0	GPIO17	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	CORESONIC_SWD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_MCU_AICE_TCKC	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TXD	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A31	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
SIM1_SCLK	0	GPIO18	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	2	MD2_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	3	MD1_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
	4	MD2_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
SIM1_SRST	0	GPIO19	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	2	MD2_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	3	MD1_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	4	MD2_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
SIM1_SIO	0	GPIO20	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM1_SIO	IO	CU, CD	4/8/12/16mA	0
	2	MD2_SIM1_SDAT	IO	CU, CD	4/8/12/16mA	0
	3	MD1_SIM2_SIO	IO	CU, CD	4/8/12/16mA	0
	4	MD2_SIM2_SDAT	IO	CU, CD	4/8/12/16mA	0
SIM2_SCLK	0	GPIO21	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
	2	MD2_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0

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	3	MD1_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	4	MD2_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
SIM2_SRST	0	GPIO22	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	2	MD2_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	3	MD1_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	4	MD2_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
SIM2_SIO	0	GPIO23	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM2_SIO	IO	CU, CD	4/8/12/16mA	0
	2	MD2_SIM2_SDAT	IO	CU, CD	4/8/12/16mA	0
	3	MD1_SIM1_SIO	IO	CU, CD	4/8/12/16mA	0
	4	MD2_SIM1_SDAT	IO	CU, CD	4/8/12/16mA	0
AUD_CLK_MOSI	0	GPIO24	IO	CU, CD	2/4/6/8mA	0
	1	AUD_CLK_MOSI	O	CU, CD	2/4/6/8mA	0
AUD_DAT_MISO	0	GPIO25	IO	CU, CD	2/4/6/8mA	0
	1	AUD_DAT_MISO	I	CU, CD	2/4/6/8mA	0
	2	VOW_DAT_MISO	I	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MOSI	O	CU, CD	2/4/6/8mA	0
AUD_DAT_MOSI	0	GPIO26	IO	CU, CD	2/4/6/8mA	0
	1	AUD_DAT_MOSI	O	CU, CD	2/4/6/8mA	0
	2	VOW_DAT_MISO	I	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MISO	I	CU, CD	2/4/6/8mA	0
DISP_PWM	0	GPIO27	IO	CU, CD	2/4/6/8mA	0
	1	DISP_PWM	O	CU, CD	2/4/6/8mA	0
LCM_RST	0	GPIO28	IO	CU, CD	2/4/6/8mA	0
	1	LCM_RST	O	CU, CD	2/4/6/8mA	0
DSI_TE	0	GPIO29	IO	CU, CD	2/4/6/8mA	0
	1	DSI_TE	I	CU, CD	2/4/6/8mA	0
CAM_CLK0	0	GPIO30	IO	CU, CD	2/4/6/8mA	0
	1	CMMCLK0	O	CU, CD	2/4/6/8mA	0
	3	TDD_TCK	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_TCK	I	CU, CD	2/4/6/8mA	0
	6	MD32_TCK	I	CU, CD	2/4/6/8mA	0
	7	MD32_JTAG_TCK	I	CU, CD	2/4/6/8mA	0
CAM_RST0	0	GPIO31	IO	CU, CD	2/4/6/8mA	0
	1	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	3	TDD_TMS	I	CU, CD	2/4/6/8mA	0
	4	EINT26	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_TMS	I	CU, CD	2/4/6/8mA	0
	6	MD32_TMS	I	CU, CD	2/4/6/8mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	7	MD32_JTAG_TMS	I	CU, CD	2/4/6/8mA	0
CAM_RST1	0	GPIO32	IO	CU, CD	2/4/6/8mA	0
	1	PWM_C	O	CU, CD	2/4/6/8mA	0
	2	AGPS_SYNC	O	CU, CD	2/4/6/8mA	0
	3	TDD_TDI	I	CU, CD	2/4/6/8mA	0
	4	EINT27	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_TDI	I	CU, CD	2/4/6/8mA	0
	6	MD32_TDI	I	CU, CD	2/4/6/8mA	0
	7	MD32_JTAG_TDI	I	CU, CD	2/4/6/8mA	0
CAM_PDN0	0	GPIO33	IO	CU, CD	2/4/6/8mA	0
	1	UCTS2	I	CU, CD	2/4/6/8mA	0
	2	UCTS3	I	CU, CD	2/4/6/8mA	0
	3	TDD_TDO	IO	CU, CD	2/4/6/8mA	0
	4	EINT28	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_TDO	O	CU, CD	2/4/6/8mA	0
	6	MD32_TDO	IO	CU, CD	2/4/6/8mA	0
	7	MD32_JTAG_TDO	IO	CU, CD	2/4/6/8mA	0
CAM_PDN1	0	GPIO34	IO	CU, CD	2/4/6/8mA	0
	1	URTS2	O	CU, CD	2/4/6/8mA	0
	2	URTS3	O	CU, CD	2/4/6/8mA	0
	3	TDD_TRSTN	I	CU, CD	2/4/6/8mA	0
	4	EINT29	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_TRST_B	I	CU, CD	2/4/6/8mA	0
	6	MD32_TRSTN	I	CU, CD	2/4/6/8mA	0
	7	MD32_JTAG_TRST	I	CU, CD	2/4/6/8mA	0
CMPCLK	0	GPIO35	IO	CU, CD	2/4/6/8mA	0
	1	CMPCLK	I	CU, CD	2/4/6/8mA	0
	2	CMCSK	I	CU, CD	2/4/6/8mA	0
	3	TDD_TXD	O	CU, CD	2/4/6/8mA	0
	4	EINT0	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_DBGI_N	I	CU, CD	2/4/6/8mA	0
	6	MD_CLKM0	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A12	IO	CU, CD	2/4/6/8mA	0
CMDAT0	0	GPIO36	IO	CU, CD	2/4/6/8mA	0
	1	CMDAT0	I	CU, CD	2/4/6/8mA	0
	2	CMCSD0	I	CU, CD	2/4/6/8mA	0
	3	PTA_RXD	I	CU, CD	2/4/6/8mA	0
	4	EINT1	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_DBGACK_N	O	CU, CD	2/4/6/8mA	0
	6	MD_CLKM1	O	CU, CD	2/4/6/8mA	0

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	7	DBG_MON_A13	IO	CU, CD	2/4/6/8mA	0
CMDAT1	0	GPIO37	IO	CU, CD	2/4/6/8mA	0
	1	CMDAT1	I	CU, CD	2/4/6/8mA	0
	2	CMCSD1	I	CU, CD	2/4/6/8mA	0
	3	PTA_TXD	O	CU, CD	2/4/6/8mA	0
	4	EINT2	I	CU, CD	2/4/6/8mA	0
	5	CONN_MCU_AICE_TMSC	IO	CU, CD	2/4/6/8mA	0
	6	CMFLASH	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A14	IO	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_CK	0	GPIO38	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPI0_CK	O	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_CSN	0	GPIO39	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPI0_CSN	O	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_MI	0	GPIO40	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPI0_MI	IO	CU, CD	2/4/6/8mA	0
	3	PWRAP_SPI0_MO	IO	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_MO	0	GPIO41	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPI0_MO	IO	CU, CD	2/4/6/8mA	0
	3	PWRAP_SPI0_MI	IO	CU, CD	2/4/6/8mA	0
WATCHDOG	0	GPIO42	IO	CU, CD	2/4/6/8mA	0
	1	WATCHDOG	O	CU, CD	2/4/6/8mA	0
SRCLKENA0	0	GPIO43	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENA0	O	CU, CD	2/4/6/8mA	0
SRCLKENA1	0	GPIO44	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENA1	O	CU, CD	2/4/6/8mA	0
SCL0	0	GPIO45	IO	CD		0
	1	SCL0_0	IO	CD		0
SCL1	0	GPIO46	IO	CD		0
	1	SCL1_0	IO	CD		0
SCL2	0	GPIO47	IO	CU, CD	2/4/6/8mA	0
	2	SCL3_1	IO	CU, CD	2/4/6/8mA	0
SCL3	0	GPIO48	IO	CD		0
	2	SCL2_1	IO	CD		0
SDA0	0	GPIO49	IO	CD		0
	1	SDA0_0	IO	CD		0
SDA1	0	GPIO50	IO	CD		0
	1	SDA1_0	IO	CD		0
SDA2	0	GPIO51	IO	CU, CD	2/4/6/8mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU /CD	Driving	SMT
	2	SDA3_1	IO	CU, CD	2/4/6/8mA	0
SDA3	0	GPIO52	IO	CD		0
	2	SDA2_1	IO	CD		0
RFIC0_BSI_EN	0	GPIO53	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_EN	O	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC0_BSI_CK	0	GPIO54	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_CK	O	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_CK	O	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D0	0	GPIO55	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_D0	IO	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D1	0	GPIO56	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D1	IO	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_D1	IO	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D2	0	GPIO57	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_D2	IO	CU, CD	2/4/6/8mA	0
RFIC1_BSI_EN	0	GPIO58	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_EN	O	CU, CD	2/4/6/8mA	0
	2	PCM1_CLK	IO	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_EN	O	CU, CD	2/4/6/8mA	0
	4	EINT30	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A21	IO	CU, CD	2/4/6/8mA	0
RFIC1_BSI_CK	0	GPIO59	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_CK	O	CU, CD	2/4/6/8mA	0
	2	PCM1_SYNC	IO	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_CK	O	CU, CD	2/4/6/8mA	0
	4	EINT31	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A22	IO	CU, CD	2/4/6/8mA	0
RFIC1_BSI_D0	0	GPIO60	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	2	PCM1_DI	I	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	4	EINT32	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A23	IO	CU, CD	2/4/6/8mA	0
RFIC1_BSI_D1	0	GPIO61	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D1	IO	CU, CD	2/4/6/8mA	0
	2	PCM1_DO	O	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_D1	IO	CU, CD	2/4/6/8mA	0
	4	EINT33	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A24	IO	CU, CD	2/4/6/8mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
RFIC1_BSI_D2	0	GPIO62	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	2	UTXD2	O	CU, CD	2/4/6/8mA	0
	3	MD2_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	4	EINT34	I	CU, CD	2/4/6/8mA	0
	5	URXD2	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A25	IO	CU, CD	2/4/6/8mA	0
MISC_BSI_CK	0	GPIO63	IO	CU, CD	2/4/6/8mA	0
	1	MISC_BSI_CK	O	CU, CD	2/4/6/8mA	0
MISC_BSI_DO	0	GPIO64	IO	CU, CD	2/4/6/8mA	0
	1	MISC_BSI_DO	IO	CU, CD	2/4/6/8mA	0
MISC_BSI_DI	0	GPIO65	IO	CU, CD	2/4/6/8mA	0
	1	MISC_BSI_DI	IO	CU, CD	2/4/6/8mA	0
	3	MIPI1_SDATA	IO	CU, CD	2/4/6/8mA	0
MISC_BSI_CS0B	0	GPIO66	IO	CU, CD	2/4/6/8mA	0
	1	MISC_BSI_CS0B	O	CU, CD	2/4/6/8mA	0
	2	MISC_BSI_CS1B	O	CU, CD	2/4/6/8mA	0
	3	MIPI1_SCLK	O	CU, CD	2/4/6/8mA	0
MISC_BSI_CS1B	0	GPIO67	IO	CU, CD	2/4/6/8mA	0
	1	MISC_BSI_CS1B	O	CU, CD	2/4/6/8mA	0
	2	MISC_BSI_CS0B	O	CU, CD	2/4/6/8mA	0
	3	MIPI1_SCLK	O	CU, CD	2/4/6/8mA	0
BPI_BUS0	0	GPIO68	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS0	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC2_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD2_BPI_BUS0	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	EINT35	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A15	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS1	0	GPIO69	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS1	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC2_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD2_BPI_BUS1	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	EINT36	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A16	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS2	0	GPIO70	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS2	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC2_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD2_BPI_BUS2	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	EINT37	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A17	IO	CU, CD	2/4/6/8/10/12/14/16mA	0

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BPI_BUS3	0	GPIO71	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS3	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC2_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD2_BPI_BUS3	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	EINT38	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A18	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS4	0	GPIO72	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS4	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC2_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD2_BPI_BUS4	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	EINT39	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A19	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS5	0	GPIO73	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC2_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	MD2_BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	EINT40	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A20	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS6	0	GPIO74	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	2	ANT_SEL0	O	CU, CD	4/8/12/16mA	0
	3	MD2_BPI_BUS6	O	CU, CD	4/8/12/16mA	0
BPI_BUS7	0	GPIO75	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS7	O	CU, CD	4/8/12/16mA	0
	2	ANT_SEL1	O	CU, CD	4/8/12/16mA	0
	3	MD2_BPI_BUS7	O	CU, CD	4/8/12/16mA	0
BPI_BUS8	0	GPIO76	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS8	O	CU, CD	4/8/12/16mA	0
	2	ANT_SEL2	O	CU, CD	4/8/12/16mA	0
	3	MD2_BPI_BUS8	O	CU, CD	4/8/12/16mA	0
BPI_BUS9	0	GPIO77	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS9	O	CU, CD	4/8/12/16mA	0
	3	MD2_BPI_BUS9	O	CU, CD	4/8/12/16mA	0
BPI_BUS10	0	GPIO78	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS10	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS10	O	CU, CD	2/4/6/8mA	0
BPI_BUS11	0	GPIO79	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS11	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS11	O	CU, CD	2/4/6/8mA	0
BPI_BUS12	0	GPIO80	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS12	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS12	O	CU, CD	2/4/6/8mA	0

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BPI_BUS13	0	GPIO81	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS13	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS13	O	CU, CD	2/4/6/8mA	0
BPI_BUS14	0	GPIO82	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS14	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS14	O	CU, CD	2/4/6/8mA	0
BPI_BUS15	0	GPIO83	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS15	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS15	O	CU, CD	2/4/6/8mA	0
BPI_BUS16	0	GPIO84	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS16	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS16	O	CU, CD	2/4/6/8mA	0
BPI_BUS17	0	GPIO85	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS17	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS17	O	CU, CD	2/4/6/8mA	0
BPI_BUS18	0	GPIO86	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS18	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS18	O	CU, CD	2/4/6/8mA	0
BPI_BUS19	0	GPIO87	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS19	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS19	O	CU, CD	2/4/6/8mA	0
BPI_BUS20	0	GPIO88	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS20	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS20	O	CU, CD	2/4/6/8mA	0
BPI_BUS21	0	GPIO89	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS21	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS21	O	CU, CD	2/4/6/8mA	0
BPI_BUS22	0	GPIO90	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS22	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS22	O	CU, CD	2/4/6/8mA	0
BPI_BUS23	0	GPIO91	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS23	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS23	O	CU, CD	2/4/6/8mA	0
BPI_BUS24	0	GPIO92	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS24	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS24	O	CU, CD	2/4/6/8mA	0
BPI_BUS25	0	GPIO93	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS25	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS25	O	CU, CD	2/4/6/8mA	0
BPI_BUS26	0	GPIO94	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS26	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS26	O	CU, CD	2/4/6/8mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
BPI_BUS27	0	GPIO95	IO	CU, CD	2/4/6/8mA	0
	1	BPI_BUS27	O	CU, CD	2/4/6/8mA	0
	3	MD2_BPI_BUS27	O	CU, CD	2/4/6/8mA	0
LTE_TXBPI	0	GPIO96	IO	CU, CD	2/4/6/8mA	0
	1	RF_DCCAL_RESULT_IN	I	CU, CD	2/4/6/8mA	0
TD_TXBPI	0	GPIO97	IO	CU, CD	2/4/6/8mA	0
	1	RF_DCCAL_RESULT_IN_OGT	I	CU, CD	2/4/6/8mA	0
	2	URXD2	I	CU, CD	2/4/6/8mA	0
	4	EINT41	I	CU, CD	2/4/6/8mA	0
	5	UTXD2	O	CU, CD	2/4/6/8mA	0
WB_CTRL0	0	GPIO98	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	WB_CTRL0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC3_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
WB_CTRL1	0	GPIO99	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	WB_CTRL1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC3_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
WB_CTRL2	0	GPIO100	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	WB_CTRL2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC3_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
WB_CTRL3	0	GPIO101	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	WB_CTRL3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC3_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
WB_CTRL4	0	GPIO102	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	WB_CTRL4	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC3_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A4	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
WB_CTRL5	0	GPIO103	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	WB_CTRL5	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	MSDC3_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_A5	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
F2W_DATA	0	GPIO104	IO	CU, CD	2/4/6/8mA	0
	1	F2W_DATA	I	CU, CD	2/4/6/8mA	0
	2	MRG_CLK	O	CU, CD	2/4/6/8mA	0
	3	PCM0_CLK	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A6	IO	CU, CD	2/4/6/8mA	0
F2W_CLK	0	GPIO105	IO	CU, CD	2/4/6/8mA	0

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	1	F2W_CLK	I	CU, CD	2/4/6/8mA	0
	2	MRG_DI	I	CU, CD	2/4/6/8mA	0
	3	PCM0_DI	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A7	IO	CU, CD	2/4/6/8mA	0
WB_SCLK	0	GPIO106	IO	CU, CD	2/4/6/8mA	0
	1	WB_SCLK	O	CU, CD	2/4/6/8mA	0
	2	MRG_DO	O	CU, CD	2/4/6/8mA	0
	3	PCM0_DO	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A8	IO	CU, CD	2/4/6/8mA	0
WB_SDATA	0	GPIO107	IO	CU, CD	2/4/6/8mA	0
	1	WB_SDATA	IO	CU, CD	2/4/6/8mA	0
	2	MRG_SYNC	O	CU, CD	2/4/6/8mA	0
	3	PCM0_SYNC	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A9	IO	CU, CD	2/4/6/8mA	0
WB_SEN	0	GPIO108	IO	CU, CD	2/4/6/8mA	0
	1	WB_SEN	O	CU, CD	2/4/6/8mA	0
	2	UTXD3	O	CU, CD	2/4/6/8mA	0
	3	URXD3	I	CU, CD	2/4/6/8mA	0
	4	TP_UTXD3_AO	O	CU, CD	2/4/6/8mA	0
	5	TP_URXD3_AO	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A10	IO	CU, CD	2/4/6/8mA	0
WB_RSTB	0	GPIO109	IO	CU, CD	2/4/6/8mA	0
	1	WB_RSTB	O	CU, CD	2/4/6/8mA	0
	2	URXD3	I	CU, CD	2/4/6/8mA	0
	3	UTXD3	O	CU, CD	2/4/6/8mA	0
	4	TP_URXD3_AO	I	CU, CD	2/4/6/8mA	0
	5	TP_UTXD3_AO	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A11	IO	CU, CD	2/4/6/8mA	0
KPCOL0	0	GPIO110	IO	CU, CD	2/4/6/8mA	0
	1	KPCOL0	IO	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A32	IO	CU, CD	2/4/6/8mA	0
KPCOL1	0	GPIO111	IO	CU, CD	2/4/6/8mA	0
	1	KPCOL1	IO	CU, CD	2/4/6/8mA	0
	2	SCL2_2	IO	CU, CD	2/4/6/8mA	0
	3	SCL3_2	IO	CU, CD	2/4/6/8mA	0
	4	DBG_SCL	IO	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B30	IO	CU, CD	2/4/6/8mA	0
KPROW0	0	GPIO112	IO	CU, CD	2/4/6/8mA	0
	1	KPROW0	IO	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B31	IO	CU, CD	2/4/6/8mA	0
KPROW1	0	GPIO113	IO	CU, CD	2/4/6/8mA	0
	1	KPROW1	IO	CU, CD	2/4/6/8mA	0

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	2	SDA2_2	IO	CU, CD	2/4/6/8mA	0
	3	SDA3_2	IO	CU, CD	2/4/6/8mA	0
	4	DBG_SDA	IO	CU, CD	2/4/6/8mA	0
	5	TP_GPIO0_AO	IO	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B32	IO	CU, CD	2/4/6/8mA	0
DPI_D0	0	GPIO114	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D0	O	CU, CD	4/8/12/16mA	0
	2	SCL1_1	IO	CU, CD	4/8/12/16mA	0
	3	SCL3_3	IO	CU, CD	4/8/12/16mA	0
	4	EINT3	I	CU, CD	4/8/12/16mA	0
	5	TP_GPIO1_AO	IO	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B8	IO	CU, CD	4/8/12/16mA	0
DPI_D1	0	GPIO115	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D1	O	CU, CD	4/8/12/16mA	0
	2	SDA1_1	IO	CU, CD	4/8/12/16mA	0
	3	SDA3_3	IO	CU, CD	4/8/12/16mA	0
	4	EINT4	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B9	IO	CU, CD	4/8/12/16mA	0
DPI_D2	0	GPIO116	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D2	O	CU, CD	4/8/12/16mA	0
	2	UCTS1	I	CU, CD	4/8/12/16mA	0
	4	EINT5	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B10	IO	CU, CD	4/8/12/16mA	0
DPI_D3	0	GPIO117	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D3	O	CU, CD	4/8/12/16mA	0
	2	URTS1	O	CU, CD	4/8/12/16mA	0
	4	EINT6	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B11	IO	CU, CD	4/8/12/16mA	0
DPI_D4	0	GPIO118	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D4	O	CU, CD	4/8/12/16mA	0
	2	SPI2_CSB	O	CU, CD	4/8/12/16mA	0
	4	EINT7	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B12	IO	CU, CD	4/8/12/16mA	0
DPI_D5	0	GPIO119	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D5	O	CU, CD	4/8/12/16mA	0
	2	SPI2_CLK	O	CU, CD	4/8/12/16mA	0
	3	ANT_SEL3	O	CU, CD	4/8/12/16mA	0
	4	EINT8	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B13	IO	CU, CD	4/8/12/16mA	0
DPI_D6	0	GPIO120	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D6	O	CU, CD	4/8/12/16mA	0
	2	SPI2_MO	O	CU, CD	4/8/12/16mA	0

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	3	ANT_SEL4	O	CU, CD	4/8/12/16mA	0
	4	EINT50	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B14	IO	CU, CD	4/8/12/16mA	0
DPI_D7	0	GPIO121	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D7	O	CU, CD	4/8/12/16mA	0
	2	SPI2_MI	I	CU, CD	4/8/12/16mA	0
	3	ANT_SEL5	O	CU, CD	4/8/12/16mA	0
	4	EINT54	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B15	IO	CU, CD	4/8/12/16mA	0
DPI_D8	0	GPIO122	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D8	O	CU, CD	4/8/12/16mA	0
	2	I2S2_MCK	O	CU, CD	4/8/12/16mA	0
	3	AUD_DAT_MISO_SPK_A	I	CU, CD	4/8/12/16mA	0
	4	EINT42	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B16	IO	CU, CD	4/8/12/16mA	0
DPI_D9	0	GPIO123	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D9	O	CU, CD	4/8/12/16mA	0
	2	I2S2_BCK	O	CU, CD	4/8/12/16mA	0
	3	MD_CDMA_GPS_SYNC	I	CU, CD	4/8/12/16mA	0
	4	EINT43	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B17	IO	CU, CD	4/8/12/16mA	0
DPI_D10	0	GPIO124	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D10	O	CU, CD	4/8/12/16mA	0
	2	I2S2_LRCK	O	CU, CD	4/8/12/16mA	0
	4	EINT44	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B18	IO	CU, CD	4/8/12/16mA	0
DPI_D11	0	GPIO125	IO	CU, CD	4/8/12/16mA	0
	1	DPI_D11	O	CU, CD	4/8/12/16mA	0
	2	I2S2_DI	I	CU, CD	4/8/12/16mA	0
	3	SRCLKENA0	O	CU, CD	4/8/12/16mA	0
	4	EINT45	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B19	IO	CU, CD	4/8/12/16mA	0
DPI_DE	0	GPIO126	IO	CU, CD	4/8/12/16mA	0
	1	DPI_DE	O	CU, CD	4/8/12/16mA	0
	2	I2S3_MCK	O	CU, CD	4/8/12/16mA	0
	3	AUD_DAT_MISO_SPK_A	I	CU, CD	4/8/12/16mA	0
	4	EINT46	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B20	IO	CU, CD	4/8/12/16mA	0
DPI_CK	0	GPIO127	IO	CU, CD	4/8/12/16mA	0
	1	DPI_CK	O	CU, CD	4/8/12/16mA	0

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	2	I2S3_BCK	O	CU, CD	4/8/12/16mA	0
	4	EINT47	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B21	IO	CU, CD	4/8/12/16mA	0
DPI_HSYNC	0	GPIO128	IO	CU, CD	4/8/12/16mA	0
	1	DPI_HSYNC	O	CU, CD	4/8/12/16mA	0
	2	I2S3_LRCK	O	CU, CD	4/8/12/16mA	0
	3	DBG_SCL	IO	CU, CD	4/8/12/16mA	0
	4	EINT48	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B22	IO	CU, CD	4/8/12/16mA	0
DPI_VSYNC	0	GPIO129	IO	CU, CD	4/8/12/16mA	0
	1	DPI_VSYNC	O	CU, CD	4/8/12/16mA	0
	2	I2S3_DO	O	CU, CD	4/8/12/16mA	0
	3	DBG_SDA	IO	CU, CD	4/8/12/16mA	0
	4	EINT49	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B23	IO	CU, CD	4/8/12/16mA	0
I2S0_MCK	0	GPIO130	IO	CU, CD	2/4/6/8mA	0
	1	I2S0_MCK	O	CU, CD	2/4/6/8mA	0
	2	URXD2	I	CU, CD	2/4/6/8mA	0
	3	UTXD2	O	CU, CD	2/4/6/8mA	0
	4	EINT11	I	CU, CD	2/4/6/8mA	0
	5	PTA_RXD	I	CU, CD	2/4/6/8mA	0
	6	AUD_DAT_MISO_SPK_B	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B0	IO	CU, CD	2/4/6/8mA	0
I2S0_BCK	0	GPIO131	IO	CU, CD	2/4/6/8mA	0
	1	I2S0_BCK	IO	CU, CD	2/4/6/8mA	0
	2	UTXD2	O	CU, CD	2/4/6/8mA	0
	3	URXD2	I	CU, CD	2/4/6/8mA	0
	4	EINT12	I	CU, CD	2/4/6/8mA	0
	5	PTA_TXD	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B1	IO	CU, CD	2/4/6/8mA	0
I2S0_LRCK	0	GPIO132	IO	CU, CD	2/4/6/8mA	0
	1	I2S0_LRCK	IO	CU, CD	2/4/6/8mA	0
	2	MD_INT2	I	CU, CD	2/4/6/8mA	0
	4	EINT13	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B2	IO	CU, CD	2/4/6/8mA	0
I2S0_DI	0	GPIO133	IO	CU, CD	2/4/6/8mA	0
	1	I2S0_DI	I	CU, CD	2/4/6/8mA	0
	2	AGPS_SYNC	O	CU, CD	2/4/6/8mA	0
	3	SRCLKENA0	O	CU, CD	2/4/6/8mA	0
	4	EINT14	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B3	IO	CU, CD	2/4/6/8mA	0

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I2S1_MCK	0	GPIO134	IO	CU, CD	2/4/6/8mA	0
	1	I2S1_MCK	O	CU, CD	2/4/6/8mA	0
	2	URXD0	I	CU, CD	2/4/6/8mA	0
	3	UTXD0	O	CU, CD	2/4/6/8mA	0
	4	EINT9	I	CU, CD	2/4/6/8mA	0
	6	AUD_DAT_MISO_SPK_B	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B4	IO	CU, CD	2/4/6/8mA	0
I2S1_BCK	0	GPIO135	IO	CU, CD	2/4/6/8mA	0
	1	I2S1_BCK	O	CU, CD	2/4/6/8mA	0
	2	UTXD0	O	CU, CD	2/4/6/8mA	0
	3	URXD0	I	CU, CD	2/4/6/8mA	0
	4	EINT51	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B5	IO	CU, CD	2/4/6/8mA	0
I2S1_LRCK	0	GPIO136	IO	CU, CD	2/4/6/8mA	0
	1	I2S1_LRCK	O	CU, CD	2/4/6/8mA	0
	2	URXD1	I	CU, CD	2/4/6/8mA	0
	3	UTXD1	O	CU, CD	2/4/6/8mA	0
	4	EINT15	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B6	IO	CU, CD	2/4/6/8mA	0
I2S1_DO	0	GPIO137	IO	CU, CD	2/4/6/8mA	0
	1	I2S1_DO	O	CU, CD	2/4/6/8mA	0
	2	UTXD1	O	CU, CD	2/4/6/8mA	0
	3	URXD1	I	CU, CD	2/4/6/8mA	0
	4	EINT52	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B7	IO	CU, CD	2/4/6/8mA	0
SRCLKENAI	0	GPIO138	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENAI	I	CU, CD	2/4/6/8mA	0
	2	UTXD3	O	CU, CD	2/4/6/8mA	0
	3	URXD3	I	CU, CD	2/4/6/8mA	0
	4	EINT53	I	CU, CD	2/4/6/8mA	0
	5	PTA_RXD	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B24	IO	CU, CD	2/4/6/8mA	0
PWM_A	0	GPIO139	IO	CU, CD	2/4/6/8mA	0
	1	PWM_A	O	CU, CD	2/4/6/8mA	0
	2	URXD3	I	CU, CD	2/4/6/8mA	0
	3	UTXD3	O	CU, CD	2/4/6/8mA	0
	4	EINT10	I	CU, CD	2/4/6/8mA	0
	5	PTA_TXD	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B25	IO	CU, CD	2/4/6/8mA	0
INT_SIM1	0	GPIO140	IO	CU, CD	4/8/12/16mA	0
	1	MD_INT0	I	CU, CD	4/8/12/16mA	0

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	2	ANT_SEL1	O	CU, CD	4/8/12/16mA	0
	4	EINT16	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B26	IO	CU, CD	4/8/12/16mA	0
INT_SIM2	0	GPIO141	IO	CU, CD	4/8/12/16mA	0
	1	MD_INT1	I	CU, CD	4/8/12/16mA	0
	2	ANT_SEL2	O	CU, CD	4/8/12/16mA	0
	4	EINT17	I	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B27	IO	CU, CD	4/8/12/16mA	0
IDDIG	0	GPIO142	IO	CU, CD	2/4/6/8mA	0
	1	IDDIG	I	CU, CD	2/4/6/8mA	0
	2	KPCOL2	IO	CU, CD	2/4/6/8mA	0
	3	UCTS0	I	CU, CD	2/4/6/8mA	0
	4	EINT18	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B28	IO	CU, CD	2/4/6/8mA	0
DRVBUS	0	GPIO143	IO	CU, CD	2/4/6/8mA	0
	1	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	0
	2	KPROW2	IO	CU, CD	2/4/6/8mA	0
	3	URTS0	O	CU, CD	2/4/6/8mA	0
	4	EINT19	I	CU, CD	2/4/6/8mA	0
	7	DBG_MON_B29	IO	CU, CD	2/4/6/8mA	0
SPI_CSB	0	GPIO144	IO	CU, CD	2/4/6/8mA	0
	1	SPI_CSB	O	CU, CD	2/4/6/8mA	0
	2	I2S2_MCK	O	CU, CD	2/4/6/8mA	0
	3	PWM_B	O	CU, CD	2/4/6/8mA	0
	4	EINT20	I	CU, CD	2/4/6/8mA	0
	5	I2S3_MCK	O	CU, CD	2/4/6/8mA	0
	6	MD_URXD	I	CU, CD	2/4/6/8mA	0
	7	JTMS_SEL1	IO	CU, CD	2/4/6/8mA	0
SPI_CLK	0	GPIO145	IO	CU, CD	2/4/6/8mA	0
	1	SPI_CLK	O	CU, CD	2/4/6/8mA	0
	2	I2S2_BCK	O	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MISO_SPK_C	I	CU, CD	2/4/6/8mA	0
	4	EINT21	I	CU, CD	2/4/6/8mA	0
	5	I2S3_BCK	O	CU, CD	2/4/6/8mA	0
	6	MD_UTXD	O	CU, CD	2/4/6/8mA	0
	7	JTCK_SEL1	I	CU, CD	2/4/6/8mA	0
SPI_MO	0	GPIO146	IO	CU, CD	2/4/6/8mA	0
	1	SPI_MO	O	CU, CD	2/4/6/8mA	0
	2	I2S2_LRCK	O	CU, CD	2/4/6/8mA	0
	3	SPI_MI	I	CU, CD	2/4/6/8mA	0
	4	EINT22	I	CU, CD	2/4/6/8mA	0

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	5	I2S3_LRCK	O	CU, CD	2/4/6/8mA	0
	6	LTE_URXD	I	CU, CD	2/4/6/8mA	0
	7	JTDI_SEL1	I	CU, CD	2/4/6/8mA	0
SPI_MI	0	GPIO147	IO	CU, CD	2/4/6/8mA	0
	1	SPI_MI	I	CU, CD	2/4/6/8mA	0
	2	I2S2_DI	I	CU, CD	2/4/6/8mA	0
	3	SPI_MO	O	CU, CD	2/4/6/8mA	0
	4	EINT23	I	CU, CD	2/4/6/8mA	0
	5	I2S3_DO	O	CU, CD	2/4/6/8mA	0
	6	LTE_UTXD	O	CU, CD	2/4/6/8mA	0
	7	JTDO_SEL1	O	CU, CD	2/4/6/8mA	0
VOW_CLK_MISO	0	GPIO148	IO	CU, CD	2/4/6/8mA	0
	1	VOW_CLK_MISO	I	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MISO_SPK_B	I	CU, CD	2/4/6/8mA	0
RDN0	0	GPIO149	I	-	-	-
	1	MIPI_RDN0	AIO	-	-	-
RDP0	0	GPIO150	I	-	-	-
	1	MIPI_RDP0	AIO	-	-	-
RDN1	0	GPIO151	I	-	-	-
	1	MIPI_RDN1	AIO	-	-	-
RDP1	0	GPIO152	I	-	-	-
	1	MIPI_RDP1	AIO	-	-	-
RCN	0	GPIO153	I	-	-	-
	1	MIPI_RCN	AIO	-	-	-
RCP	0	GPIO154	I	-	-	-
	1	MIPI_RCP	AIO	-	-	-
RDN2	0	GPIO155	I	-	-	-
	1	MIPI_RDN2	AIO	-	-	-
RDP2	0	GPIO156	I	-	-	-
	1	MIPI_RDP2	AIO	-	-	-
RDN3	0	GPIO157	I	-	-	-
	1	MIPI_RDN3	AIO	-	-	-
RDP3	0	GPIO158	I	-	-	-
	1	MIPI_RDP3	AIO	-	-	-
RDN0_A	0	GPIO159	I	-	-	-
	1	MIPI_RDN0_A	AIO	-	-	-
	2	CMDAT2	I	-	-	-
	3	CMCSD2	I	-	-	-
RDP0_A	0	GPIO160	I	-	-	-
	1	MIPI_RDP0_A	AIO	-	-	-

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	2	CMDAT3	I	-	-	-
	3	CMCSD3	I	-	-	-
RDN1_A	0	GPIO161	I	-	-	-
	1	MIPI_RDN1_A	AIO	-	-	-
	2	CMDAT4	I	-	-	-
RDP1_A	0	GPIO162	I	-	-	-
	1	MIPI_RDP1_A	AIO	-	-	-
	2	CMDAT5	I	-	-	-
RCN_A	0	GPIO163	I	-	-	-
	1	MIPI_RCN_A	AIO	-	-	-
	2	CMHSYNC	I	-	-	-
RCP_A	0	GPIO164	I	-	-	-
	1	MIPI_RCP_A	AIO	-	-	-
	2	CMVSYNC	I	-	-	-
RDN2_A	0	GPIO165	I	-	-	-
	1	MIPI_RDN2_A	AIO	-	-	-
	2	CMDAT6	I	-	-	-
RDP2_A	0	GPIO166	I	-	-	-
	1	MIPI_RDP2_A	AIO	-	-	-
	2	CMDAT7	I	-	-	-
RDN3_A	0	GPIO167	I	-	-	-
	1	MIPI_RDN3_A	AIO	-	-	-
	2	CMDAT8	I	-	-	-
RDP3_A	0	GPIO168	I	-	-	-
	1	MIPI_RDP3_A	AIO	-	-	-
	2	CMDAT9	I	-	-	-
TDN3	0	GPIO169	I	-	-	-
	1	MIPI_TDN3	AIO	-	-	-
TDP3	0	GPIO170	I	-	-	-
	1	MIPI_TDP3	AIO	-	-	-
TDN2	0	GPIO171	I	-	-	-
	1	MIPI_TDN2	AIO	-	-	-
TDP2	0	GPIO172	I	-	-	-
	1	MIPI_TDP2	AIO	-	-	-
TCN	0	GPIO173	I	-	-	-
	1	MIPI_TCN	AIO	-	-	-
TCP	0	GPIO174	I	-	-	-
	1	MIPI_TCP	AIO	-	-	-
TDN1	0	GPIO175	I	-	-	-
	1	MIPI_TDN1	AIO	-	-	-
TDP1	0	GPIO176	I	-	-	-
	1	MIPI_TDP1	AIO	-	-	-

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Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
TDN0	0	GPIO177	I	-	-	-
	1	MIPI_TDN0	AIO	-	-	-
TDP0	0	GPIO178	I	-	-	-
	1	MIPI_TDP0	AIO	-	-	-
GPS_RXQN	0	GPIO179	I	-	-	-
	1	GPS_RXQN	AIO	-	-	-
	4	EINT55	I	-	-	-
GPS_RXQP	0	GPIO180	I	-	-	-
	1	GPS_RXQP	AIO	-	-	-
	4	EINT56	I	-	-	-
GPS_RXIN	0	GPIO181	I	-	-	-
	1	GPS_RXIN	AIO	-	-	-
	4	EINT57	I	-	-	-
GPS_RXIP	0	GPIO182	I	-	-	-
	1	GPS_RXIP	AIO	-	-	-
	4	EINT58	I	-	-	-
WB_RXQN	0	GPIO183	I	-	-	-
	1	WB_RXQN	AIO	-	-	-
	4	EINT59	I	-	-	-
WB_RXQP	0	GPIO184	I	-	-	-
	1	WB_RXQP	AIO	-	-	-
	4	EINT60	I	-	-	-
WB_RXIN	0	GPIO185	I	-	-	-
	1	WB_RXIN	AIO	-	-	-
	4	EINT61	I	-	-	-
WB_RXIP	0	GPIO186	I	-	-	-
	1	WB_RXIP	AIO	-	-	-
	4	EINT62	I	-	-	-

Table 7. Pin multiplexing, capability and settings

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD18_PLLGP AVDD18_MEMPLL AVDD18_MDPLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
DVDD18_MIPITX1	Analog power for MIPI DSI	1.7	1.9	V
DVDD18_MIPIRX0 DVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.7	1.9	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.7	1.9	V
DVDD18_IO1 DVDD18_IO2 DVDD18_IO3 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3	Digital power input for 1.8V IO	1.62	1.98	V
DVDD28_BPI1 DVDD28_BPI2	Digital power input for BPI	1.7	3.6	V
DVDD18_MSDC0	Digital power input for MSDC0	1.62	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	3.6	V
DVDD28_MD	Digital power input for MD INT	1.7	2.94	V
DVDD28_SIM1	Digital power input for SIM1	1.7	3.6	V
DVDD28_SIM2	Digital power input for SIM2	1.7	3.6	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for DRAM	1.14	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.72	1.131	V
DVDD_GPU	Digital power input for GPU	0.93	1.125	V
DVDD_LTE	Digital power input for LTE	0.9	1.1	V
DVDD_SRAM	Digital power input for SRAM	0.93	1.131	V
DVDD_TOP	Digital power input for TOP	0.63	1.125	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

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2.2.2 Recommended Operating Conditions

Table 9. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_PLLGP AVDD18_MEMPLL AVDD18_MDPLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
DVDD18_MIPITX1	Analog power for MIPI DSI	1.71	1.8	1.89	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power for MIPI CSI0 & CSI1	1.71	1.8	1.89	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD28_BPI1 DVDD28_BPI2	Digital power input for BPI	1.7	1.8	1.95	V
		2.66	2.8	2.94	
DVDD18_IO1 DVDD18_IO2 DVDD18_IO3 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.62	1.8	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD28_MD	Digital power input for MD INT	1.7	1.8	1.95	V
		2.66	2.8	2.94	
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7	3.3	3.6	V
		1.7	1.8	1.9	
DDRV DDRV_CLK DDRV_VREF	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.72	1.0	1.131	V
DVDD_GPU	Digital power input for GPU	0.93	1.0	1.125	V
DVDD_LTE	Digital power input for LTE	0.9	1.0	1.1	V
DVDD_SRAM	Digital power input for SRAM	0.93	1.0	1.131	V
DVDD_TOP	Digital power input for TOP	0.63	1.0	1.125	V

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:

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- Mounted within 168 hours in factory condition of 30°C/60% RH, or
- Stored at 20% RH

3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 5. Basic timing parameter for LPDDR3 commands, Figure 6 and Figure 7, is used to connect LPDDR3 device for MT6752. It includes pins CLK_T, CLK_C, CKE[1:0], CS[1:0], DQS[3:0], DQS#[3:0], CA[9:0] and DQ[31:0]. Table 10 summarizes the symbol definition and the related timing specifications.

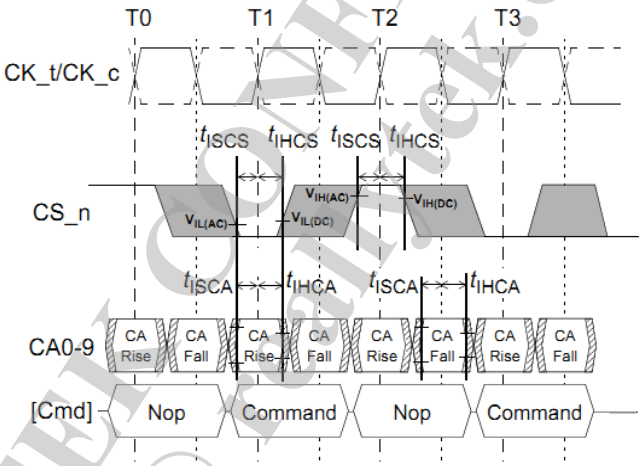

Figure 5. Basic timing parameter for LPDDR3 commands

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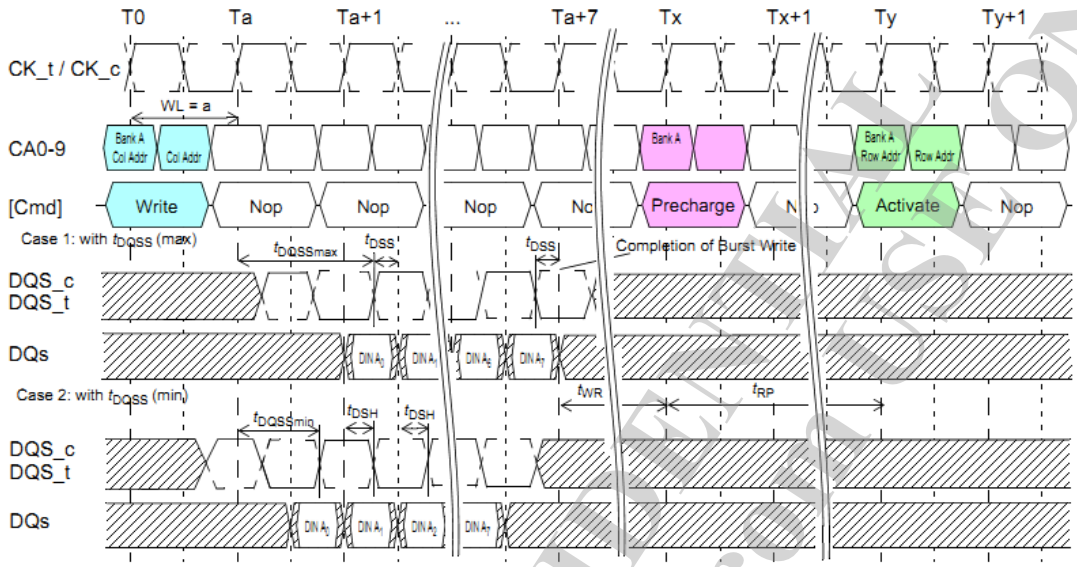

Figure 6. Basic timing parameter for LPDDR3 write

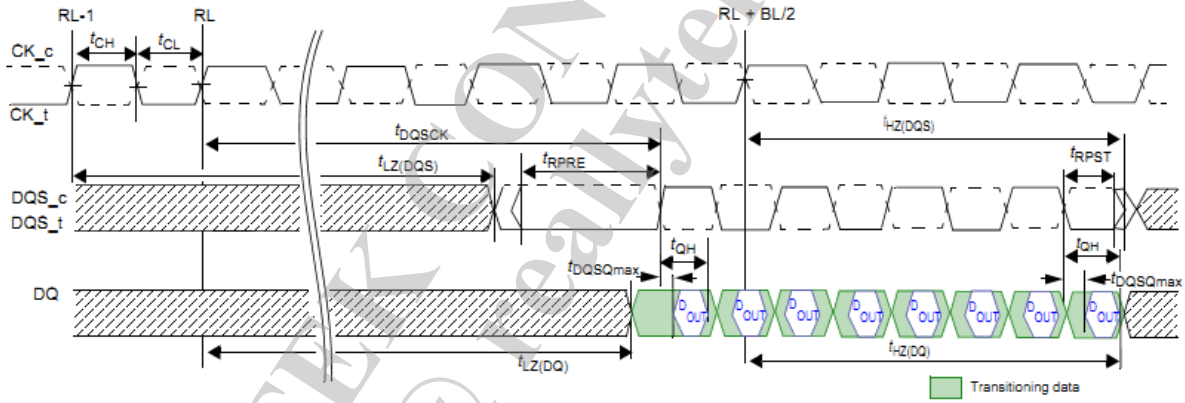

Figure 7. Basic LPDDR3 read timing parameter

Table 10. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK

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Symbol	Description	Min.	Typ.	Max.	Unit
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	Max. (7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'			tDQSCK (MAX) – 0.1	ns
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'			tDQSCK (MAX) + [1.4*tDQSQ (MAX)]	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	Min. (tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max. (10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max. (10tCK, 14)			ns
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max. (42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-charge)			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max. (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max. (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max. (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max. (10ns, 2tCK)			ns
tWR	WRITE recovery time	Max. (15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max. (7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max. (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max. (7.5ns, 3tCK)			ns
tREFW	Refresh period			32	ms
tRFCab	Refresh cycle time	130			ns
tRFCpb	Per bank refresh cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max. (7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

2.2.4.2 External Memory Interface for LPDDR2

The external memory interface, shown in Figure 5. Basic timing parameter for LPDDR3 commands, Figure 69 and Figure 710, is used to connect LPDDR2 device for MT6752. It includes pins ED_CLK, ED_CLK_B, ECKE, ECS#, EBA[2:0], EDQS[3:0], EDQS#[3:0], EA[9:0] and ED[31:0]. Table 10 summarizes the symbol definition and the related timing specifications.

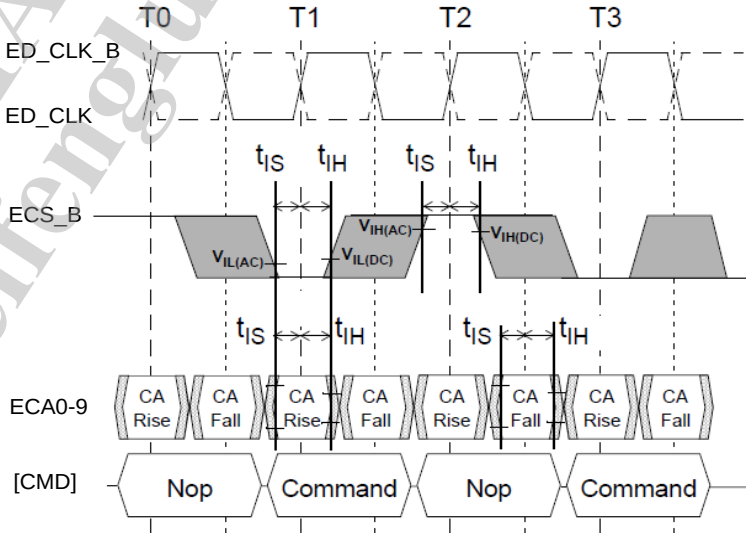

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Figure 8. Basic timing parameter for LPDDR2 commands

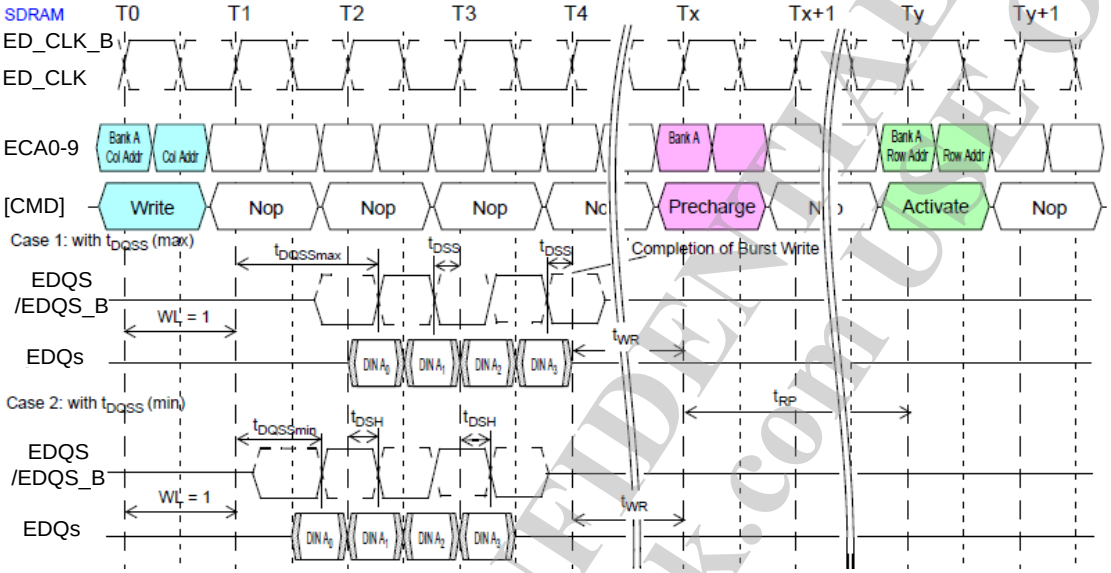

Figure 9. Basic timing parameter for LPDDR2 write

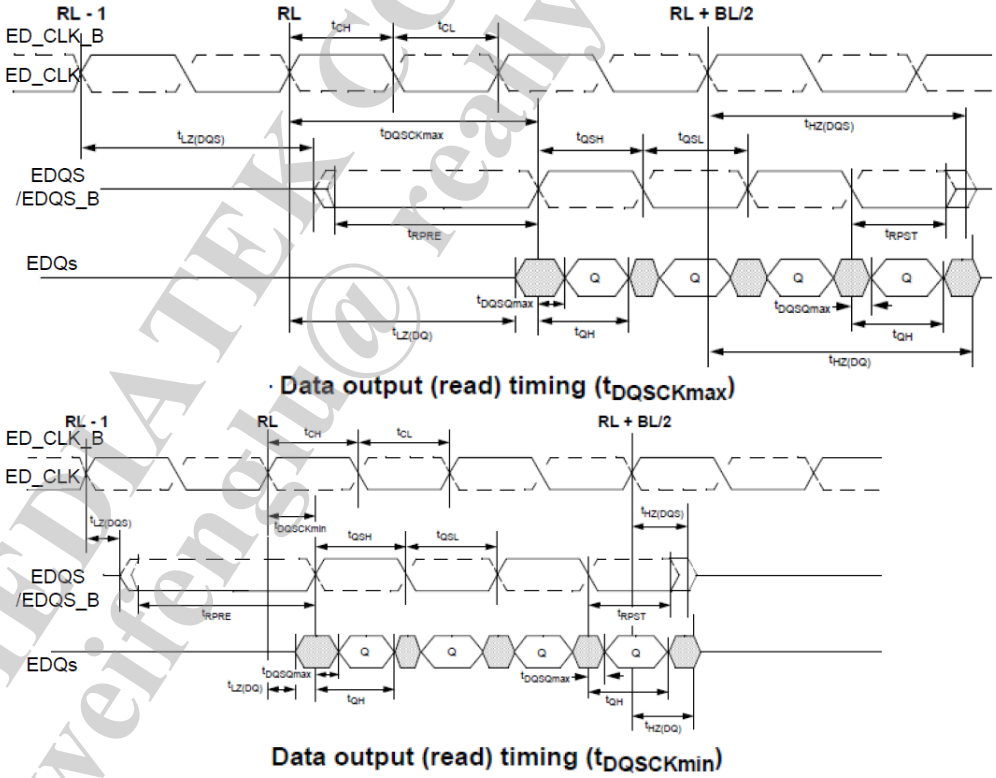

Figure 10. Basic timing parameter for LPDDR2 read

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Table 11. LPDDR2 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	3.75		8	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.43			ns
tDH	DQ & DM input hold time	0.43			ns
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tIS	Address & control input setup time	0.46			ns
tIH	Address & control input hold time	0.46			ns
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK (Min.) – 300			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'	tDQSCK (Max.) – 100			ns
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (Min.) – [1.4*tQHS (Max.)]			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'	tDQSCK (Max.) + [1.4*tDQSQ (Max.)]			ns
tDQSQ	DQS-DQ skew	0.34			ns
tQHP	Data half period	Min. (tQSH, tQSL)			tCK
tQHS	Data hold skew factor	0.4			ns
tQH	DQ/DQS output hold time from DQS	tQHP – tQHS			ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH – 0.05			tCK
tQSL	DQS output low pulse width	tCL – 0.05			tCK
tMRW	MODE register Write command period	5			tCK
tMRR	MODE register Read command period	2			tCK
tRPRE	Read preamble	0.9		1.1	tCK
tRPST	Read postamble	tCL – 0.05			tCK
tRAS	ACTIVE to PRECHARGE command period	3			tCK
tRC	ACTIVE to ACTIVE command period	6			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			tCK
tRCD	ACTIVE to READ or WRITE delay	3			tCK
tRP	PRECHARGE command period	3			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR	WRITE recovery time	3			tCK
tWTR	Internal write to READ command time	2			tCK
tXSR	SELF REFRESH exit to the next valid command	40			tCK

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Symbol	Description	Min.	Typ.	Max.	Unit
tXP	EXIT power-down to the next valid command delay	2			tCK
tCKE	CKE min. pulse width (high & low pulse width)	2			tCK

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2.3 System Configuration

2.3.1 Mode Selection

Table 12. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI [1] PWRAP_SPI0_CSN	00: Use CAM pins for legacy JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG

2.3.2 Constant Tie Pins

Table 13. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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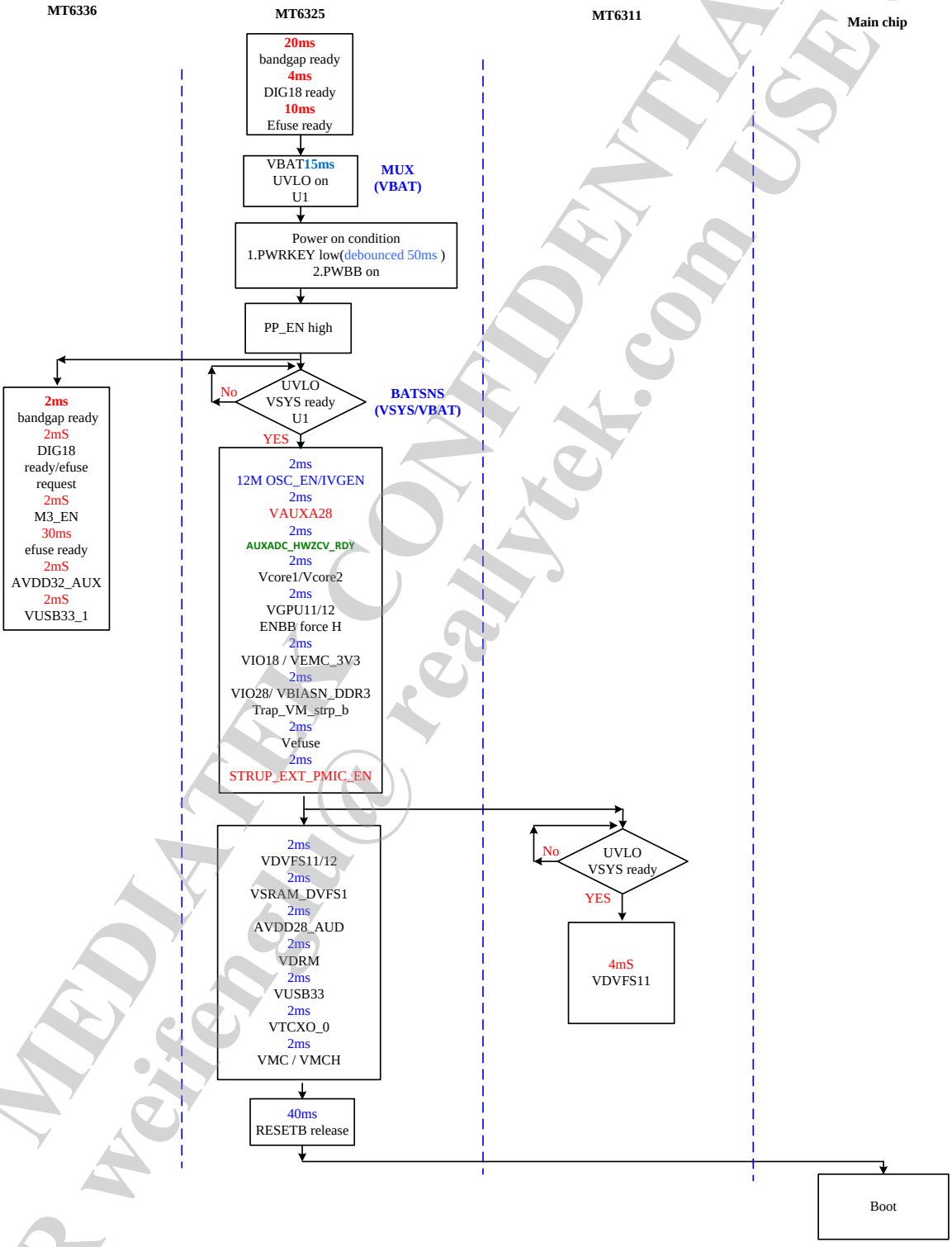
2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:



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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- RF control: Two DACs for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers respectively.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- LTE_BBRX
- TD_BBRX
- BBTX
- ETDAC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 LTE_BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.

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2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

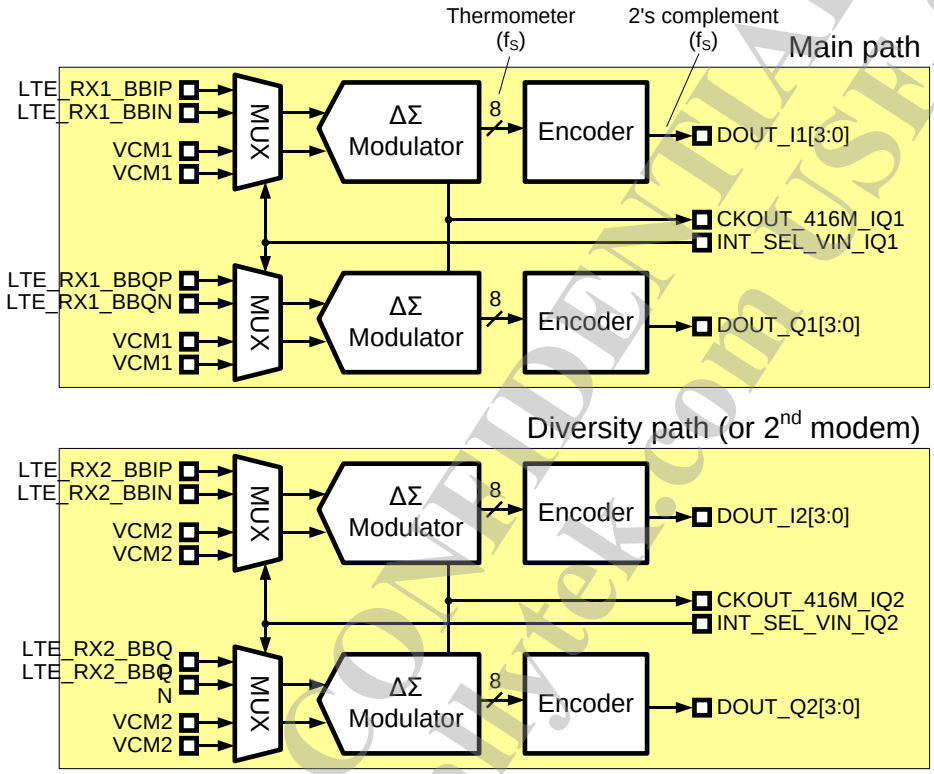

Figure 11. Block diagram of LTE_BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 14. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency – Clock rate (LTE HB mode) – Clock rate (LTE LB mode) – Clock rate (DC mode) – Clock rate (SC mode & GSM mode)		 416 208 416 208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, DC mode			0.14	% (rms)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance – LTE HB mode – LTE LB mode – DC mode – SC mode & GSM mode	 2.8 5.6 5.6 11.2	 4 8 8 16	 5.2 10.4 10.4 20.8	kΩ
FS	Output sampling rate		416/208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – LTE HB mode, 2.4Vpp (10.2MHz) sinewave, 1kHz ~ 9MHz band – LTE LB mode, 2.4Vpp (5.2MHz) sinewave, 1kHz ~ 4.5MHz band – DC mode, 2.4Vpp (5.2MHz) sinewave, 400kHz ~ 4.6MHz band – SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	 68 68 72 72 84	 71 71 75 75 87		 dB dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		80	°C
	Current consumption (per channel) – Power-up – Power-down			 4.5 1	 mA uA

2.5.3.2 TD_BBRX

2.5.3.2.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 2 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

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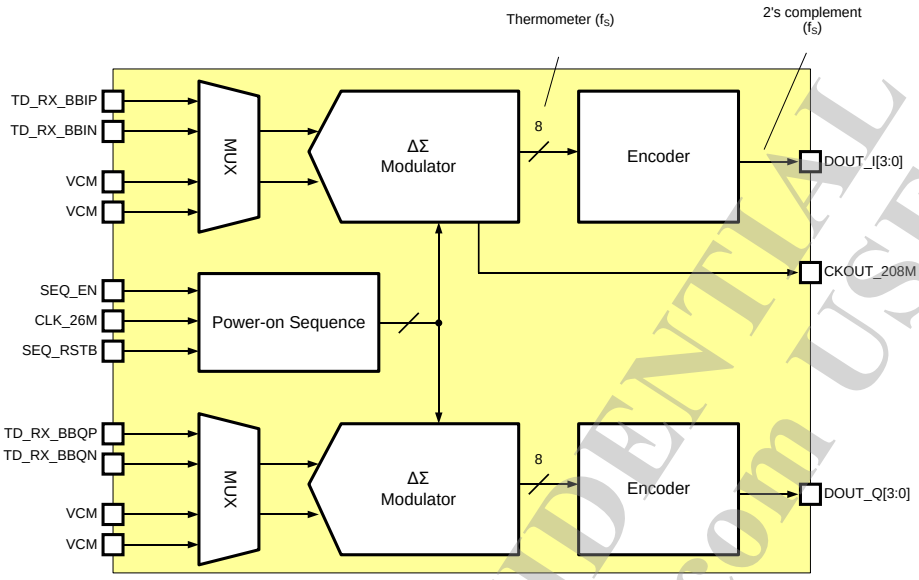

Figure 12: Block diagram of TD_BBRX-ADC

2.5.3.3 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 15: Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.7	0.75	0.8	V
FC	Clock rate		208		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter			0.61	% (rms)
RIN	Differential input resistance	11.2	16	20.8	kΩ
FS	Output sampling rate		208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – 2.4Vpp (1.6MHz) sinewave, 1kKHz ~ 640kHz band	75	78		dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		80	°C
	Current consumption (per channel) – Power-up – Power-down			 2 1	 mA uA

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2.5.3.4 LTE_BBTX

2.5.3.4.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

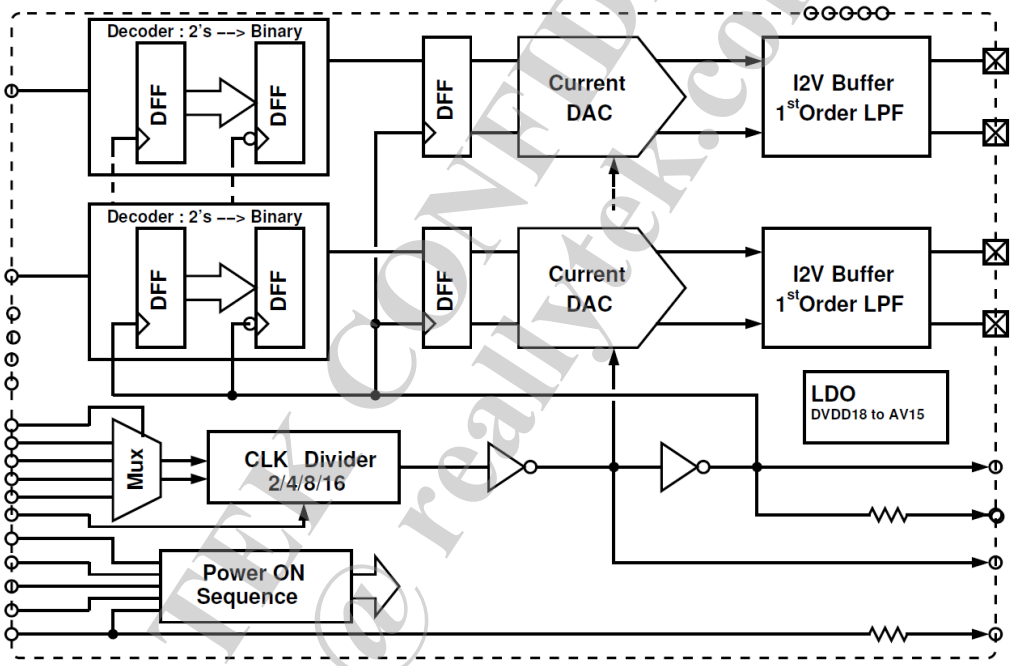

Figure 13. Block diagram of LTE_BBTX

2.5.3.4.2 Functional Specifications

Table 16. LTE_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
N_{OOB}	Output noise level @25MHz		40		nVrms/sqrt(Hz)
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 8 10		 mA uA

2.5.3.5 TD_BBTX

2.5.3.5.1 Block Descriptions

BBTX includes two channels of DACs with the first order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current, and the active RC filter performs current to the voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. MD-PLL deliver 832MHz differential clock to BBTX. A clock divider translates 832MHz to 416MHz for DACs and AFIFO inside the mixedsys.

The IO power, DVDD18_MD, is regulated to a voltage around 1.55V to supply analog component, and the required bias currents are generated by BBRX.

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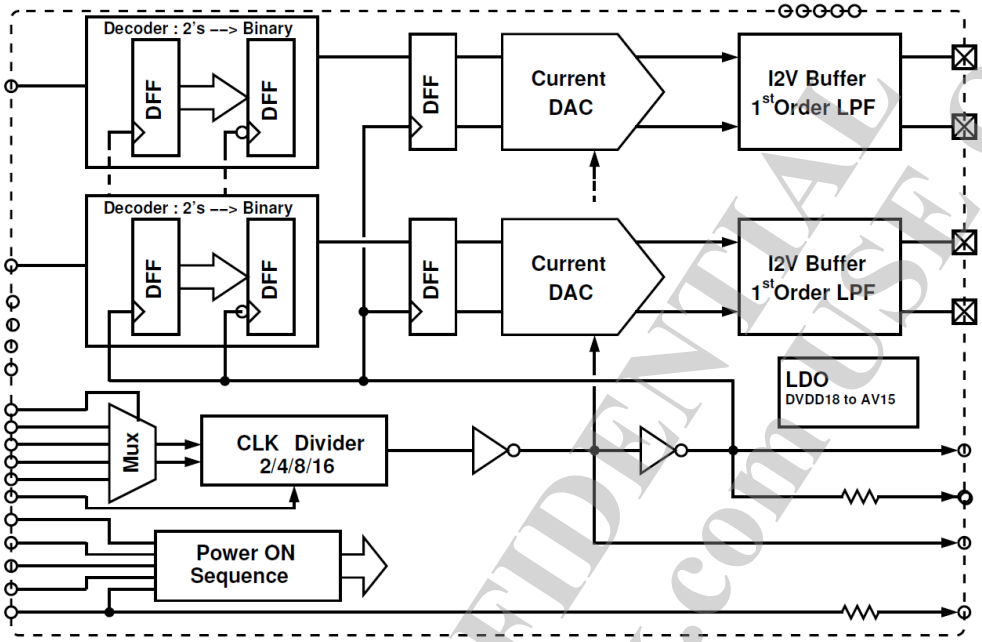

Figure 14. Block diagram of TD_BBTX

2.5.3.5.2 Functional Specifications

Table 17. TD_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit.
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF Leakage current @ supply, Irms @416*2=832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os_T}	3-sigma output differential DC offset over temp.			4	mV
V_{os}	3-sigma output differential DC offset			10	mV
F_{3dB}	3dB corner freq.	20	25	30	MHz
S_{LPF}	LPF selectivity @832MHz	28			dB
N_{OOB}	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C
	Current consumption Power-up		6.7		mA

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Symbol	Parameter	Min.	Typ.	Max.	Unit.
	Power-down		10		uA

2.5.3.6 ETDAC

2.5.3.6.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 15/30MHz 1st-order Butterworth frequency response.

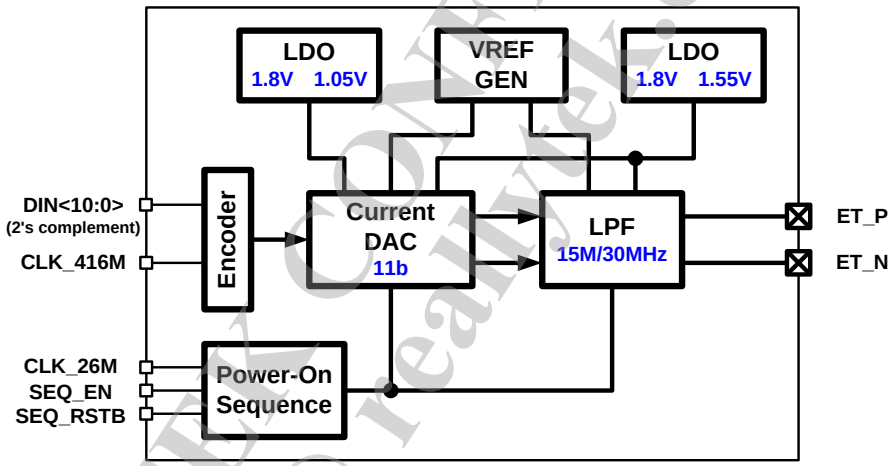

Figure 15. Block diagram of ETDAC

2.5.3.6.2 Functional Specfications

Table 18. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
FCUT	Filter -3dB cutoff frequency (calibrated)		15/30		MHz
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.7 APC-DAC

2.5.3.7.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

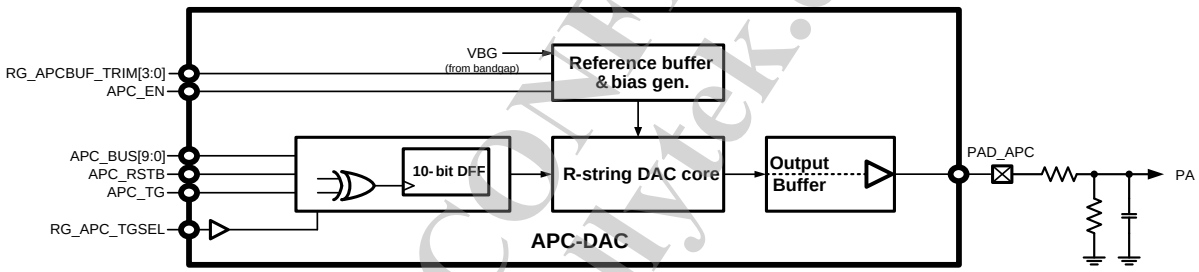

Figure 16. Block diagram of APC-DAC

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 19. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
Fs	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
Ts	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		450		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.8 AUXADC

2.5.3.8.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

See
Table 20. Definitions of AUXADC channels for brief descriptions of AUXADC input channels.

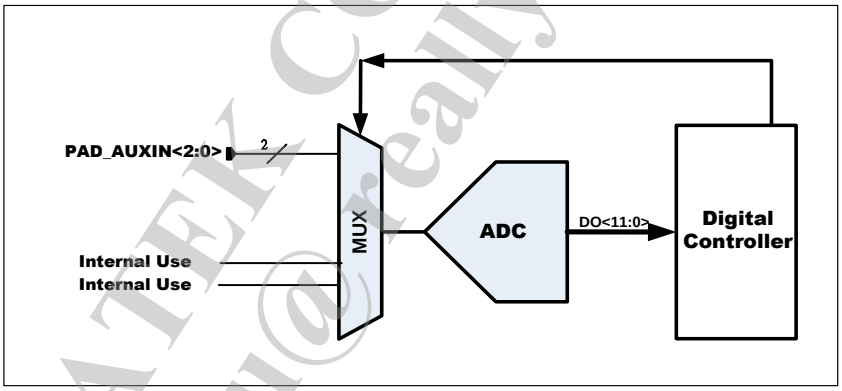

Figure 17. Block diagram of AUXADC

Table 20. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	NA
Channel 3	NA
Channel 4	NA
Channel 5	NA
Channel 6	NA

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AUXADC channel ID	Description
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	Internal use
Channel 11	Internal use
Channel 12	External use (AUX_IN2)
Channel 13	NA
Channel 14	NA
Channel 15	NA

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 21. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	20			 MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	62	68		dB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.75	1.8	1.85	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 400 1		 uA uA

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2.5.3.9 Clock Squarer

2.5.3.9.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.9.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 22. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		500		uA

2.5.3.10 Phase Locked Loop

2.5.3.10.1 Block Descriptions

There are total 17 PLLs in PLL macro separated into 2 groups, providing several clocks for CPU, BUS, modem, analog modem, MSDC and image-sensor.

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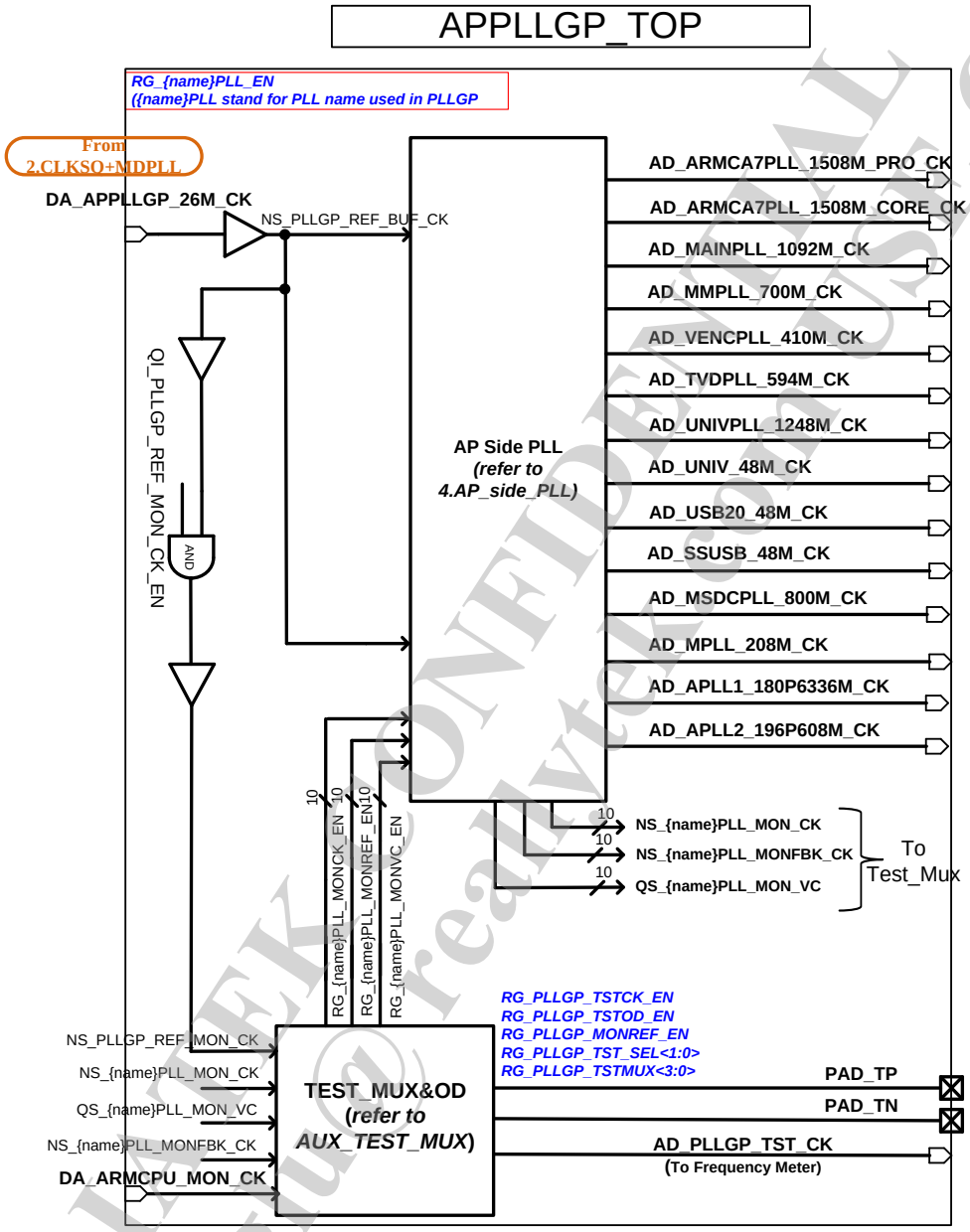

Figure 18. Block diagram of APPLLGP

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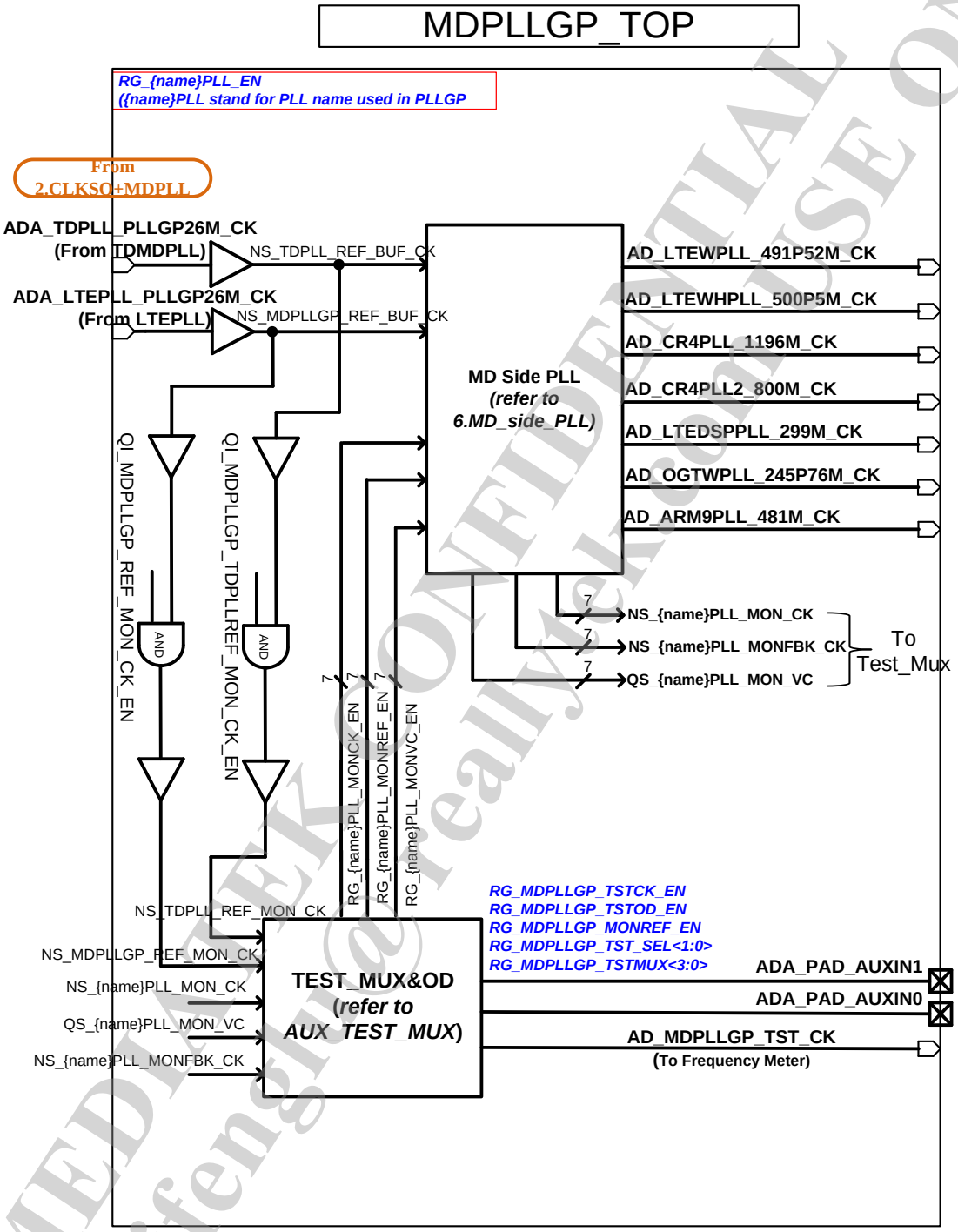

Figure 19. Block diagram of MDPLLGP

2.5.3.10.2 Functional Specifications

See the table below for the functional specifications of PLL.

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Table 23. ARMCA7PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1508		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 24. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1.2		mA
	Power-down current consumption			0.1	uA

Table 25. MMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		700		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 26. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	1248	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 27. MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		800		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 28. MDPLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		100		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (rms period jitter)		1.59		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		4.2		mA
	Power-down current consumption			0.3	uA

Table 29. MDPLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	416	N/A	MHz
	Settling time		100		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (rms period jitter)		2.52		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		2.5		mA
	Power-down current consumption			0.2	uA

Table 30. LTEWPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	491.52	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 31. LTEWHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		500.5		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 32. CR4PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency		1196		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 33. VENCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		410		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 34. TVDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		594		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 35. CR4PLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		800		MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 36. OGTWPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		245.76		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 37. LTEDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		299		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 38. MPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		208		MHz
	Settling time		20		Us

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 39. APLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		180.6336		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 40. APLL2 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		196.608		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

Table 41. ARM9PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		481		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.81	1.0	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			0.1	uA

2.5.3.11 Temperature Sensor

2.5.3.11.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.11.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 42. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

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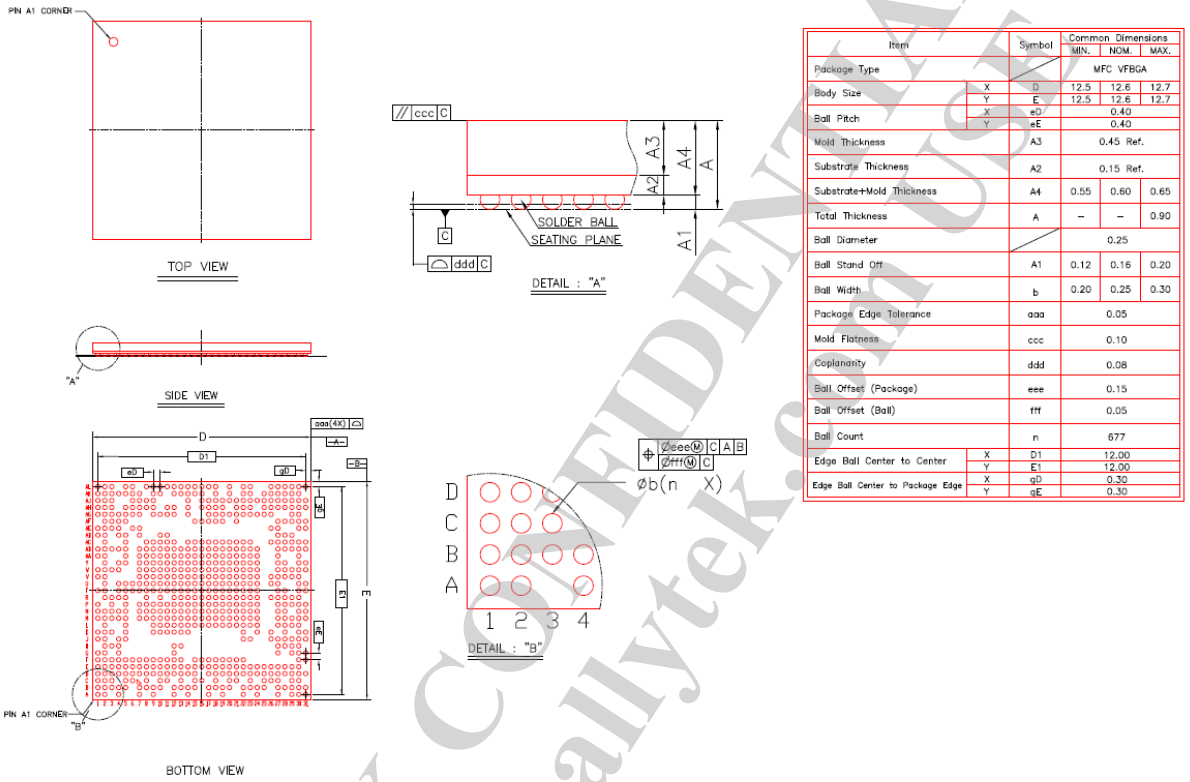
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.5	12.6	12.7
	Y	E	12.5	12.6	12.7
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.45 Ref.	
Substrate Thickness		A2		0.15 Ref.	
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.90
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		677	
Edge Ball Center to Center	X	D1		12.00	
	Y	E1		12.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 20. Outlines and dimensions of TFBGA 12.6mm*12.6mm, 677-ball, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 43. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	37.65	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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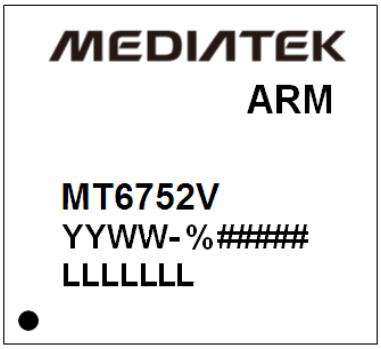
2.7 Ordering Information

2.7.1 Top Marking Definition



- YYWW: Date code
- %: Functional code
  - L: FDD LTE/TDD LTE/UMTS/TDSCDMA/GSM
  - C: TDD LTE/TDSCDMA/GSM
- #####: Subcontractor code
- LLLLLLL: Die lot No.

Figure 21. Top mark of MT6752

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